TC1796

32-Bit Single-Chip Microcontroller

TriCore

Microcontrollers

Never stop thinking

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TC1796 Data Sheet

Revision History: V1.0, 2008-04

Previous Version: V1.0, 2008-04 “Preliminary”	
Page	Subjects (major changes since last revision)
	“Preliminary” status removed. No changes in content.
Changes from V0.7, 2006-03 to V1.0, 2008-04 Preliminary	
32	The list of not connected pins (N.C.) improved by adding several formerly as V_{SS} labeled pins.
69	Watchdog timer, double reset detection, description corrected.
80	RTID register updated for the design step BE.
85	The description of the inactive device current improved.
96	ADC parameters sample and conversion time moved to a dedicated table.
107	The description of the power supply sequence improved..
115	BFCLKO clock, duty cycle description extended.
126	MLI timing, maximum operating frequency limit extended, t31 added.
131	The drawing of the package updated. Green package variant included.
133	Example of a temperature profile corrected.

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1 Summary of Features

- High-performance 32-bit super-scalar TriCore V1.3 CPU with 4-stage pipeline
  - Superior real-time performance
  - Strong bit handling
  - Fully integrated DSP capabilities
  - Single precision Floating Point Unit (FPU)
  - 150 MHz operation at full temperature range
- 32-bit Peripheral Control Processor with single cycle instruction (PCP2)
  - 16 Kbyte Parameter Memory (PRAM)
  - 32 Kbyte Code Memory (CMEM)
- Multiple on-chip memories
  - 2 Mbyte Program Flash Memory (PFLASH) with ECC
  - 128 Kbyte Data Flash Memory (DFLASH) usable for EEPROM emulation
  - 136 Kbyte Data Memory (LDRAM, SRAM, SBRAM)
  - 8 Kbyte Dual-Ported Memory (DPRAM)
  - 48 Kbyte Code Scratchpad Memory (SPRAM)
  - 16 Kbyte Instruction Cache (ICACHE)
  - 16 Kbyte BootROM (BROM)
- 16-Channel DMA Controller
- 32-bit External Bus Interface Unit (EBU) with
  - 75 dedicated address/data bus, clock, and control lines
  - Synchronous burst Flash access capability
- Sophisticated interrupt system with 2×255 hardware priority arbitration levels serviced by CPU or PCP2
- High performing on-chip bus structure
  - Two 64-bit Local Memory Buses between EBU, Flash and Data Memory
  - 32-bit System Peripheral Bus (SPB) for on-chip peripheral and functional units
  - 32-bit Remote Peripheral Bus (RPB) for high-speed on-chip peripheral units
  - Two bus bridges (LFI Bridge, DMA Controller)
- Peripheral Control Processor with single cycle instruction (PCP2)
  - 16 Kbyte Parameter Memory (PRAM)
  - 32 Kbyte Code Memory (CMEM)
- Versatile On-chip Peripheral Units
  - Two Asynchronous/Synchronous Serial Channels (ASC) with baud rate generator, parity, framing and overrun error detection
  - Two High-Speed Synchronous Serial Channels (SSC) with programmable data length and shift direction
  - Two serial Micro Second Bus interfaces (MSC) for serial port expansion to external power devices
  - Two High-Speed Micro Link interfaces (MLI) for serial inter-processor communication

  - One MultiCAN Module with four CAN nodes and 128 free assignable message objects for high efficiency data handling via FIFO buffering and gateway data transfer (one CAN node supports TTCAN functionality)
  - Two General Purpose Timer Array Modules (GPTA) with additional Local Timer Cell Array (LTCA2) providing a powerful set of digital signal filtering and timer functionality to realize autonomous and complex Input/Output management
  - Two 16-channel Analog-to-Digital Converter units (ADC) with selectable 8-bit, 10-bit, or 12-bit resolution
  - One 4-channel Fast Analog-to-Digital Converter unit (FADC) with concatenated comb filters for hardware data reduction: supporting 10-bit resolution, min. conversion time of 280ns
- 44 analog input lines for ADC and FADC
- 123 digital general purpose I/O lines, 4 input lines
- Digital I/O ports with 3.3 V capability
- On-chip debug support for OCDS Level 1 and 2 (CPU, PCP3, DMA)
- Dedicated Emulation Device chip for multi-core debugging, tracing, and calibration via USB V1.1 interface available (TC1796ED)
- Power Management System
- Clock Generation Unit with PLL
- Core supply voltage of 1.5 V
- I/O voltage of 3.3 V
- Full automotive temperature range: -40° to +125°C
- P/PG-BGA-416-4 package

Ordering Information

The ordering code for Infineon microcontrollers provides an exact reference to the required product. This ordering code identifies:

- The derivative itself, i.e. its function set, the temperature range, and the supply voltage
- The package and the type of delivery.

For the available ordering codes for the TC1796 please refer to the **“Product Catalog Microcontrollers”**, which summarizes all available microcontroller variants.

This document describes the derivatives of the device.The **Table 1** enumerates these derivatives and summarizes the differences.

Table 1 TC1796 Derivative Synopsis

Derivative	Ambient Temperature Range
SAK-TC1796-256F150E	T_A = -40°C to +125°C

2 General Device Information

2.1 TC1796 Block Diagram

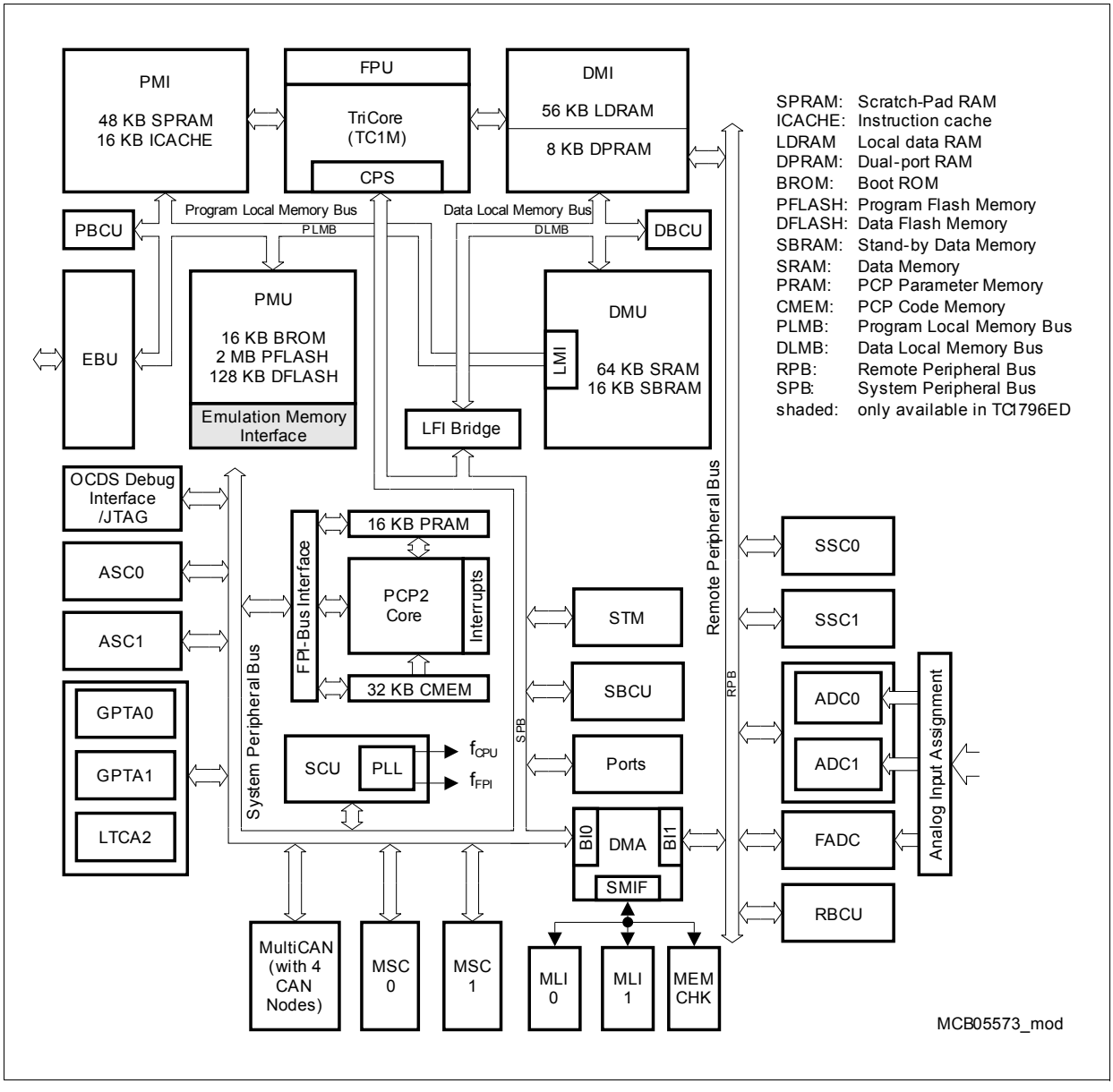


Figure 1 TC1796 Block Diagram

2.2 Logic Symbol

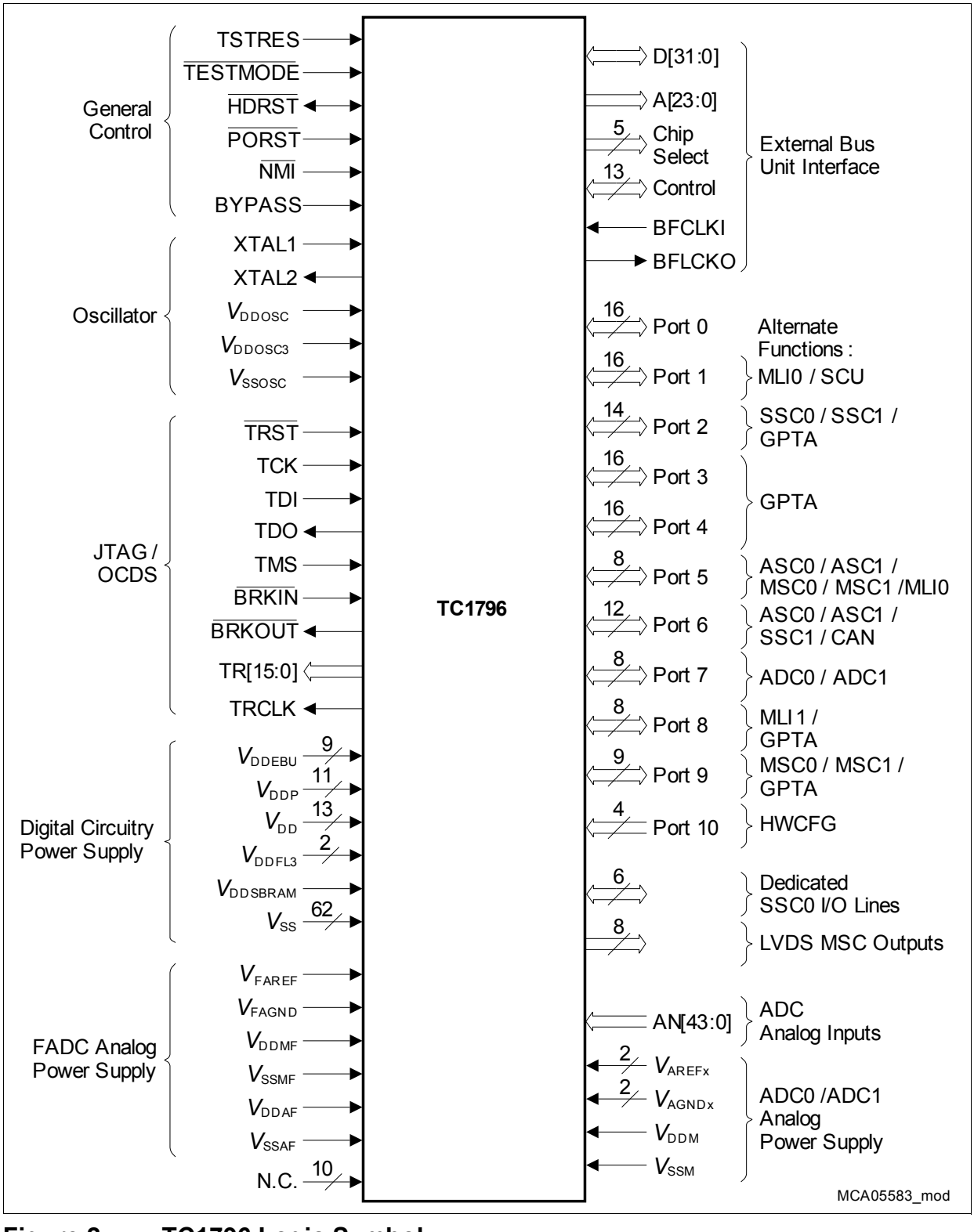


Figure 2 TC1796 Logic Symbol

2.3 Pin Configuration

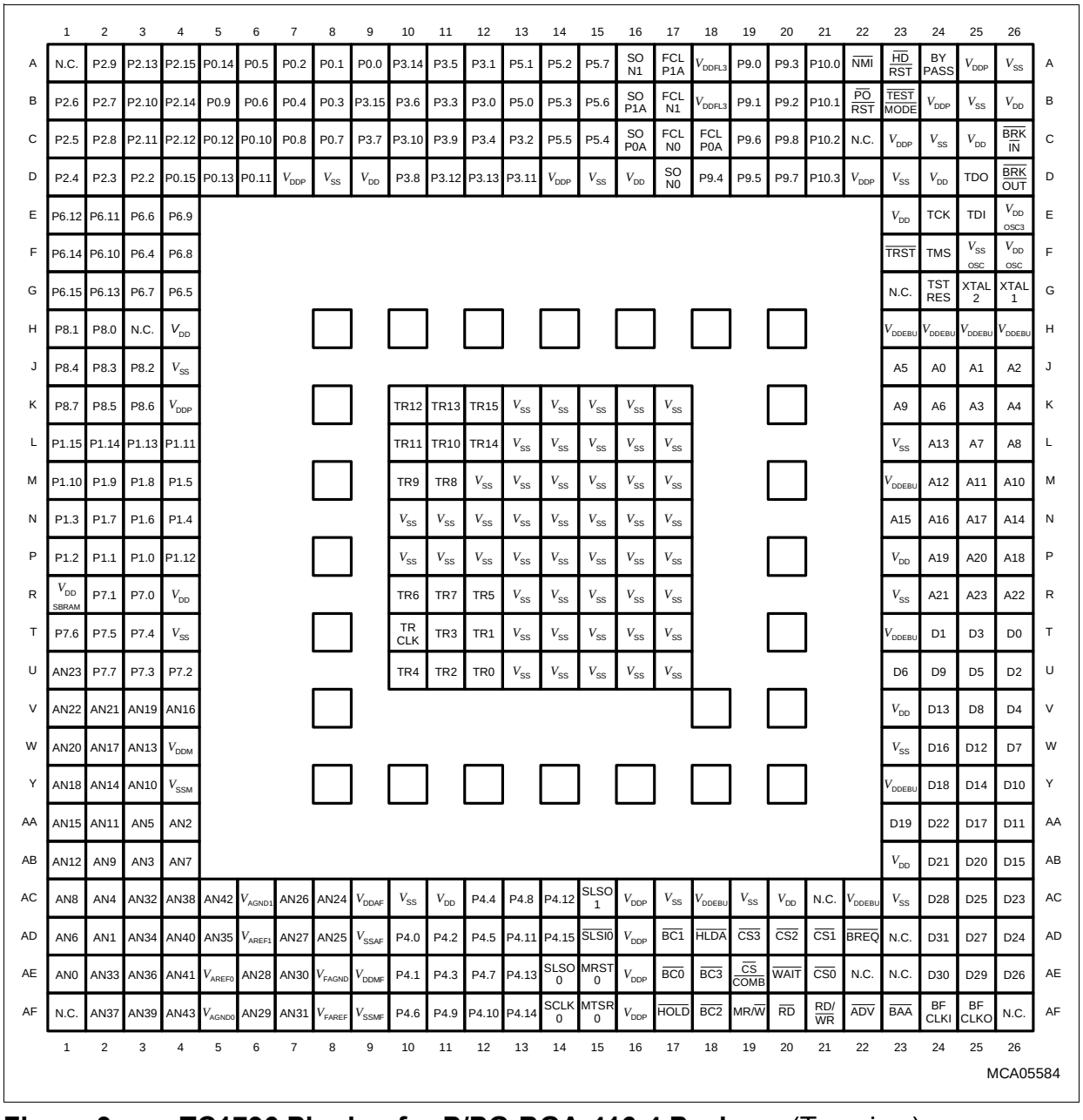


Figure 3 TC1796 Pinning for P/PG-BGA-416-4 Package (Top view)

2.4 Pad Driver and Input Classes Overview

The TC1796 provides different types and classes of input and output lines. For understanding of the abbreviations in **Table 2** starting at the next page, **Table 4** gives an overview on the pad type and class types.

2.5 Pin Definitions and Functions

Table 2 Pin Definitions and Functions

Symbol	Pins	I/O	Pad Class	Power Supply	Functions
External Bus Interface Lines (EBU)					
D[31:0]		I/O	B1	V_{DDEBU}	**EBU Data Bus Lines** The EBU Data Bus Lines D[31:0] serve as external data bus.
D0	T26	I/O			Data bus line 0
D1	T24	I/O			Data bus line 1
D2	U26	I/O			Data bus line 2
D3	T25	I/O			Data bus line 3
D4	V26	I/O			Data bus line 4
D5	U25	I/O			Data bus line 5
D6	U23	I/O			Data bus line 6
D7	W26	I/O			Data bus line 7
D8	V25	I/O			Data bus line 8
D9	U24	I/O			Data bus line 9
D10	Y26	I/O			Data bus line 10
D11	AA26	I/O			Data bus line 11
D12	W25	I/O			Data bus line 12
D13	V24	I/O			Data bus line 13
D14	Y25	I/O			Data bus line 14
D15	AB26	I/O			Data bus line 15
D16	W24	I/O			Data bus line 16
D17	AA25	I/O			Data bus line 17
D18	Y24	I/O			Data bus line 18
D19	AA23	I/O			Data bus line 19
D20	AB25	I/O			Data bus line 20
D21	AB24	I/O			Data bus line 21
D22	AA24	I/O			Data bus line 22
D23	AC26	I/O			Data bus line 23
D24	AD26	I/O			Data bus line 24
D25	AC25	I/O			Data bus line 25
D26	AE26	I/O			Data bus line 26
D27	AD25	I/O			Data bus line 27
D28	AC24	I/O			Data bus line 28
D29	AE25	I/O			Data bus line 29
D30	AE24	I/O			Data bus line 30
D31	AD24	I/O			Data bus line 31

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Class	Power Supply	Functions
A[23:0]		O	B1	V_{DDEBU}	**EBU Address Bus Lines A[23:0]** The EBU Address Bus Lines serve as external address bus.
A0	J24	O			Address bus line 0
A1	J25	O			Address bus line 1
A2	J26	O			Address bus line 2
A3	K25	O			Address bus line 3
A4	K26	O			Address bus line 4
A5	J23	O			Address bus line 5
A6	K24	O			Address bus line 6
A7	L25	O			Address bus line 7
A8	L26	O			Address bus line 8
A9	K23	O			Address bus line 9
A10	M26	O			Address bus line 10
A11	M25	O			Address bus line 11
A12	M24	O			Address bus line 12
A13	L24	O			Address bus line 13
A14	N26	O			Address bus line 14
A15	N23	O			Address bus line 15
A16	N24	O			Address bus line 16
A17	N25	O			Address bus line 17
A18	P26	O			Address bus line 18
A19	P24	O			Address bus line 19
A20	P25	O			Address bus line 20
A21	R24	O			Address bus line 21
A22	R26	O			Address bus line 22
A23	R25	O			Address bus line 23
			B1	V_{DDEBU}	**Chip Select Output Lines**
$\overline{CS0}$	AE21	O			Chip select output line 0
$\overline{CS1}$	AD21	O			Chip select output line 1
$\overline{CS2}$	AD20	O			Chip select output line 2
CS3	AD19	O			Chip select output line 3
$\overline{CS}$ COMB	AE19	O	B1	V_{DDEBU}	**Combined Chip Select Output for Global Select / Emulator Memory Region/Emulator Overlay Memory**

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Class	Power Supply	Functions
BFCLKO	AF25	O	B2	V_{DDEBU}	**Burst Mode Flash Clock Output (non-differential)**
BFCLKI	AF24	I	B1		**Burst Mode Flash Clock Input** (feedback clock)
$\overline{RD}$	AF20	O	B1		**Read Control Line**
RD/$\overline{WR}$	AF21	O	B1		**Write Control Line**
$\overline{ADV}$	AF22	O	B1		Address Valid Output
MR/$\overline{W}$	AF19	O	B1		**Motorola-style Read/Write Control Signal**
			B1		**Byte Control Lines**
$\overline{BC0}$	AE17	O			Byte control line 0
$\overline{BC1}$	AD17	O			Byte control line 1
$\overline{BC2}$	AF18	O			Byte control line 2
$\overline{BC3}$	AE18	O			Byte control line 3
$\overline{WAIT}$	AE20	I	B1		**Wait Input for inserting Wait-States**
$\overline{BAA}$	AF23	O	B1		**Burst Address Advance Output**
$\overline{HOLD}$	AF17	I	B1		**Hold Request Input**
$\overline{HLDA}$	AD18	O	B1		**Hold Acknowledge Output**
$\overline{BREQ}$	AD22	O	B1		**Bus Request Output**

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Class	Power Supply	Functions
Parallel Ports					
P0		I/O	A1	V_{DDP}	**Port 0** Port 0 is a 16-bit bidirectional general-purpose I/O port.
P0.0	A9	I/O			Port 0 I/O line 0
P0.1	A8	I/O			Port 0 I/O line 1
P0.2	A7	I/O			Port 0 I/O line 2
P0.3	B8	I/O			Port 0 I/O line 3
P0.4	B7	I/O			Port 0 I/O line 4
P0.5	A6	I/O			Port 0 I/O line 5
P0.6	B6	I/O			Port 0 I/O line 6
P0.7	C8	I/O			Port 0 I/O line 7
P0.8	C7	I/O			Port 0 I/O line 8
P0.9	B5	I/O			Port 0 I/O line 9
P0.10	C6	I/O			Port 0 I/O line 10
P0.11	D6	I/O			Port 0 I/O line 11
P0.12	C5	I/O			Port 0 I/O line 12
P0.13	D5	I/O			Port 0 I/O line 13
P0.14	A5	I/O			Port 0 I/O line 14
P0.15	D4	I/O			Port 0 I/O line 15 The states of the Port 0 pins are latched into the software configuration input register SCU_SCILR at the rising edge of $\overline{\text{HDRST}}$. Therefore, Port 0 pins can be used for operating mode selections by software.

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Class	Power Supply	Functions	
P1		I/O	A1/A2	V_{DDP}	**Port 1** Port 1 is a 16-bit bi-directional general-purpose I/O port which can be alternatively used for the MLI0 interface or as external trigger input lines.	
P1.0	P3	I	A1		REQ0	External trigger input 0
P1.1	P2	I	A1		REQ1	External trigger input 1
P1.2	P1	I	A1		REQ2	External trigger input 3
P1.3	N1	I	A1		REQ3	External trigger input 2
		I	A1		TREADY0B	MLI0 transmit channel ready input B
P1.4	N4	O	A2		TCLK0	MLI0 transmit channel clock output
P1.5	M4	I	A1		TREADY0A	MLI0 transmit channel ready input A
P1.6	N3	O	A2		TVALID0A	MLI0 transmit channel valid output A
P1.7	N2	O	A2		TDATA0	MLI0 transmit channel data output
P1.8	M3	I	A1		RCLK0A	MLI0 receive channel clock input A
P1.9	M2	O	A2		RREADY0A	MLI0 receive channel ready output A
P1.10	M1	I	A1		RVALID0A	MLI0 receive channel valid input A
P1.11	L4	I	A1		RDATA0A	MLI0 receive channel data input A
P1.12	P4	O	A2		SYSCLK	System clock output
P1.13	L3	I	A1		RCLK0B	MLI0 receive channel clock input B
P1.14	L2	I	A1		RVALID0B	MLI0 receive channel valid input B
P1.15	L1	I	A1		RDATA0B	MLI0 receive channel data input B

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Class	Power Supply	Functions
P2		I/O	A1/A2	V_{DDP}	**Port 2** Port 2 is a 14-bit bi-directional general-purpose I/O port which can be used alternatively for the six upper SSC slave select outputs or for GPTA I/O lines.
P2.2	D3	O	A2		SLSO2 Slave select output line 2
P2.3	D2	O	A2		SLSO3 Slave select output line 3
P2.4	D1	O	A2		SLSO4 Slave select output line 4
P2.5	C1	O	A2		SLSO5 Slave select output line 5
P2.6	B1	O	A2		SLSO6 Slave select output line 6
P2.7	B2	O	A2		SLSO7 Slave select output line 7
P2.8	C2	I/O	A1		IN0 / OUT0 line of GPTA
P2.9	A2	I/O	A1		IN1 / OUT1 line of GPTA
P2.10	B3	I/O	A1		IN2 / OUT2 line of GPTA
P2.11	C3	I/O	A1		IN3 / OUT3 line of GPTA
P2.12	C4	I/O	A1		IN4 / OUT4 line of GPTA
P2.13	A3	I/O	A1		IN5 / OUT5 line of GPTA
P2.14	B4	I/O	A1		IN6 / OUT6 line of GPTA
P2.15	A4	I/O	A1		IN7 / OUT7 line of GPTA

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Class	Power Supply	Functions
P3		I/O	A1	V_{DDP}	**Port 3** Port 3 is a 16-bit bi-directional general-purpose I/O port which can be alternatively used for GPTA I/O lines.
P3.0	B12				IN8 / OUT8 line of GPTA
P3.1	A12				IN9 / OUT9 line of GPTA
P3.2	C13				IN10 / OUT10 line of GPTA
P3.3	B11				IN11 / OUT11 line of GPTA
P3.4	C12				IN12 / OUT12 line of GPTA
P3.5	A11				IN13 / OUT13 line of GPTA
P3.6	B10				IN14 / OUT14 line of GPTA
P3.7	C9				IN15 / OUT15 line of GPTA
P3.9	D10				IN16 / OUT16 line of GPTA
P3.8	C11				IN17 / OUT17 line of GPTA
P3.10	C10				IN18 / OUT18 line of GPTA
P3.11	D13				IN19 / OUT19 line of GPTA
P3.12	D11				IN20 / OUT20 line of GPTA
P3.13	D12				IN21 / OUT21 line of GPTA
P3.14	A10				IN22 / OUT22 line of GPTA
P3.15.	B9				IN23 / OUT23 line of GPTA

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Class	Power Supply	Functions
P4		I/O	A1/A2	V_{DDP}	**Port 4** Port 4 is a 16-bit bi-directional general-purpose I/O port which can be alternatively used for GPTA I/O lines.
P4.0	AD10	I/O	A2[1)]		IN24 / OUT24 line of GPTA
P4.1	AE10	I/O	A2[1)]		IN25 / OUT25 line of GPTA
P4.2	AD11	I/O	A2[1)]		IN26 / OUT26 line of GPTA
P4.3	AE11	I/O	A2[1)]		IN27 / OUT27 line of GPTA
P4.4	AC12	I/O	A2[1)]		IN28 / OUT28 line of GPTA
P4.5	AD12	I/O	A2[1)]		IN29 / OUT29 line of GPTA
P4.6	AF10	I/O	A2[1)]		IN30 / OUT30 line of GPTA
P4.7	AE12	I/O	A2[1)]		IN31 / OUT31 line of GPTA
P4.8	AC13	I/O	A1		IN32 / OUT32 line of GPTA
P4.9	AF11	I/O	A1		IN33 / OUT33 line of GPTA
P4.10	AF12	I/O	A1		IN34 / OUT34 line of GPTA
P4.11	AD13	I/O	A1		IN35 / OUT35 line of GPTA
P4.12	AC14	I/O	A1		IN36 / OUT36 line of GPTA
P4.13	AE13	I/O	A1		IN37 / OUT37 line of GPTA
P4.14	AF13	I/O	A1		IN38 / OUT38 line of GPTA
P4.15	AD14	I/O	A1		IN39 / OUT39 line of GPTA

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Class	Power Supply	Functions	
P5		I/O	A2	V_{DDP}	**Port 5** Port 5 is an 8-bit bi-directional general-purpose I/O port which can be alternatively used for ASC0/1 or MSC0/1 lines.	
P5.0	B13	I/O			RXD0A	ASC0 receiver input / output A
P5.1	A13	O			TXD0A	ASC0 transmitter output A
P5.2	A14	I/O			RXD1A	ASC1 receiver input / output A
P5.3	B14	O			TXD1A	ASC1 transmitter output A P5.3 is latched with the rising edge of $\overline{\text{PORST}}$ if BYPASS = 1 and stored in inverted state as bit OSC_CON.MOSC.
P5.4	C15	O			EN00	MSC0 device select output 0
		O			RREADY0B	MLI0 receive channel ready output B
P5.5	C14	I			SDI0	MSC0 serial data input
P5.6	B15	O			EN10	MSC1 device select output 0
		O			TVALID0B	MLI0 transmit channel valid output B
P5.7	A15	I			SDI1	MSC1 serial data input

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Class	Power Supply	Functions	
P6		I/O	A2	V_{DDP}	**Port 6** Port 6 is a 12-bit bi-directional general-purpose I/O port which can be alternatively used for SSC1, ASC0/1, and CAN I/O lines.	
P6.4	F3	O I			MTSR1	SSC1 master transmit output / SSC1 slave receive input
P6.5	G4	I O			MRST1	SSC1 master receive input / SSC1 slave transmit output
P6.6	E3	I/O			SCLK1	SSC1 clock input / output
P6.7	G3	I			SLSI1	SSC1 slave select input
P6.8	F4	I I/O			RXDCAN0 RXD0B	CAN node 0 receiver input ASC0 receiver input / output B
P6.9	E4	O O			TXDCAN0 TXD0B	CAN node 0 transmitter output ASC0 transmitter output B
P6.10	F2	I I/O			RXDCAN1 RXD1B	CAN node 1 receiver input ASC1 receiver input / output B
P6.11	E2	O O			TXDCAN1 TXD1B	CAN node 1 transmitter output ASC1 transmitter output B
P6.12	E1	I			RXDCAN2	CAN node 2 receiver input
P6.13	G2	O			TXDCAN2	CAN node 2 transmitter output
P6.14	F1	I			RXDCAN3	CAN node 3 receiver input
P6.15	G1	O			TXDCAN3	CAN node 3 transmitter output

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Class	Power Supply	Functions	
P7		I/O	A1	V_{DDP}	**Port 7** Port 7 is an 8-bit bi-directional general-purpose I/O port which can be alternatively used as external trigger input lines and for ADC0/1 external multiplexer control.	
P7.0	R3	I			REQ4	External trigger input 4
P7.1	R2	I			REQ5	External trigger input 5
		O			AD0EMUX2	ADC0 external multiplexer control output 2
P7.2	U4	O			AD0EMUX0	ADC0 external multiplexer control output 0
P7.3	U3	O			AD0EMUX2	ADC0 external multiplexer control output 1
P7.4	T3	I			REQ6	External trigger input 6
P7.5	T2	I			REQ7	External trigger input 7
P7.6	T1	O			AD1EMUX0	ADC1 external multiplexer control output 0
P7.7	U2	O			AD1EMUX1	ADC1 external multiplexer control output 1

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Class	Power Supply	Functions	
P8		I/O	A1/A2	V_{DDP}	**Port 8** Port 8 is an 8-bit bi-directional general-purpose I/O port which can be alternatively used for the MLI1 interface or as GPTA I/O lines.	
P8.0	H2	O	A2		TCLK1	MLI1 transmit channel clock output
		I/O	A2		IN40/OUT40	I/O line of GPTA
P8.1	H1	I	A1		TREADY1A	MLI1 transmit channel ready input A
		I/O	A1		IN41/OUT41	I/O line of GPTA
P8.2	J3	O	A2		TVALID1A	MLI1 transmit channel valid output A
		I/O	A2		IN42/OUT42	I/O line of GPTA
P8.3	J2	O	A2		TDATA1	MLI1 transmit channel data output
		I/O	A2		IN43/OUT43	I/O line of GPTA
P8.4	J1	I	A1		RCLK1A	MLI1 receive channel clock input A
		I/O	A1		IN44/OUT44	I/O line of GPTA
P8.5	K2	O	A2		RREADY1A	MLI1 receive channel ready output A
		I/O	A2		IN45/OUT45	I/O line of GPTA
P8.6	K3	I	A1		RVALID1A	MLI1 receive channel validinput A
		I/O	A1		IN46/OUT46	I/O line of GPTA
P8.7	K1	I	A1		RDATA1A	MLI1 receive channel data input A
		I/O	A1		IN47/OUT47	I/O line of GPTA

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Class	Power Supply	Functions
P9		I/O	A2	V_{DDP}	**Port 9** Port 9 is a 9-bit bi-directional general-purpose I/O port which can be alternatively used as GPTA or MSC0/1 I/O lines.
P9.0	A19	I/O O			IN48/OUT48 I/O line of GPTA EN12 MSC1 device select output 2
P9.1	B19	I/O O			IN49/OUT49 I/O line of GPTA EN11 MSC1 device select output 1
P9.2	B20	I/O O			IN50/OUT50 I/O line of GPTA SOP1B MSC1 serial data output
P9.3	A20	I/O O			IN51/OUT51 I/O line of GPTA FCLP1 MSC1 clock output
P9.4	D18	I/O O			IN52/OUT52 I/O line of GPTA EN03 MSC0 device select output 3
P9.5	D19	I/O O			IN53/OUT53 I/O line of GPTA EN02 MSC0 device select output 2
P9.6	C19	I/O O			IN54/OUT54 I/O line of GPTA EN01 MSC0 device select output 1
P9.7	D20	I/O O			IN55/OUT55 I/O line of GPTA SOP0B MSC0 serial data output
P9.8	C20	O			FCLP0B MSC0 clock output

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Class	Power Supply	Functions
P10		I	A1	V_{DDP}	**Hardware Configuration Inputs / Port 10** These inputs are boot mode (hardware configuration) control inputs. They are latched with the rising edge of HDRST.
P10.0	A21	I			Port 10 input line 0 / HWCFG0
P10.1	B21	I			Port 10 input line 1 / HWCFG1
P10.2	C21	I			Port 10 input line 2 / HWCFG2
P10.3	D21	I			Port 10 input line 3 / HWCFG3 After reset (HDRST = 1) the state of the Port 10 input pins may be modified from the reset configuration state. There actual state can be read via software (P10_IN register). During normal operation input HWCFG1 serves as emergency shut-off control input for certain I/O lines (e.g. GPTA related outputs).
Dedicated Peripheral I/Os					
SLSO0	AE14	O	A2	V_{DDP}	**SSC0 Slave Select Output Line 0**
SLSO1	AC15	O			**SSC0 Slave Select Output Line 1**
MTSR0	AF15	O I			**SSC0 Master Transmit Output / SSC0 Slave Receive Input**
MRST0	AE15	I O			**SSC0 Master Receive Input / SSC0 Slave Transmit Output**
SCLK0	AF14	I/O			**SSC0 Clock Input/Output**
SLSI0	AD15	I			**SSC0 Slave Select Input**

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Class	Power Supply	Functions
MSC Outputs					
			C	V_{DDP}	**LVDS MSC Clock and Data Outputs**[2]
FCLP0A	C18	O			MSC0 differential driver clock output positive A
FCLN0	C17	O			MSC0 differential driver clock output negative
SOP0A	C16	O			MSC0 differential driver serial data output positive A
SON0	D17	O			MSC0 differential driver serial data output negative
FCLP1A	A17	O			MSC1 differential driver clock output positive A
FCLN1	B17	O			MSC1 differential driver clock output negative
SOP1A	B16	O			MSC1 differential driver serial data output positive A
SON1	A16	O			MSC1 differential driver serial data output negative

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Class	Power Supply	Functions
Analog Inputs					
AN[43:0]		I	D	–	**ADC Analog Input Port** The ADC Analog Input Port provides 44 analog input lines for the A/D converters ADC0, ADC1, and FADC.
AN0	AE1	I			Analog input 0
AN1	AD2	I			Analog input 1
AN2	AA4	I			Analog input 2
AN3	AB3	I			Analog input 3
AN4	AC2	I			Analog input 4
AN5	AA3	I			Analog input 5
AN6	AD1	I			Analog input 6
AN7	AB4	I			Analog input 7
AN8	AC1	I			Analog input 8
AN9	AB2	I			Analog input 9
AN10	Y3	I			Analog input 10
AN11	AA2	I			Analog input 11
AN12	AB1	I			Analog input 12
AN13	W3	I			Analog input 13
AN14	Y2	I			Analog input 14
AN15	AA1	I			Analog input 15
AN16	V4	I			Analog input 16
AN17	W2	I			Analog input 17
AN18	Y1	I			Analog input 18
AN19	V3	I			Analog input 19
AN20	W1	I			Analog input 20
AN21	V2	I			Analog input 21
AN22	V1	I			Analog input 22
AN23	U1	I			Analog input 23
AN24	AC8	I			Analog input 24
AN25	AD8	I			Analog input 25
AN26	AC7	I			Analog input 26
AN27	AD7	I			Analog input 27
AN28	AE6	I			Analog input 28
AN29	AF6	I			Analog input 29
AN30	AE7	I			Analog input 30
AN31	AF7	I			Analog input 31

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Class	Power Supply	Functions
			D	–	**ADC Analog Input Port (cont'd)**
AN32	AC3	I			Analog input 32
AN33	AE2	I			Analog input 33
AN34	AD3	I			Analog input 34
AN35	AD5	I			Analog input 35
AN36	AE3	I			Analog input 36
AN37	AF2	I			Analog input 37
AN38	AC4	I			Analog input 38
AN39	AF3	I			Analog input 39
AN40	AD4	I			Analog input 40
AN41	AE4	I			Analog input 41
AN42	AC5	I			Analog input 42
AN43	AF4	I			Analog input 43
TR[15:0]		O	A3	V_{DDP}	**OCDS Level 2 Debug Trace Lines**[2] (located on center balls)
TR0	U12	O			Trace output line 0
TR1	T12	O			Trace output line 1
TR2	U11	O			Trace output line 2
TR3	T11	O			Trace output line 3
TR4	U10	O			Trace output line 4
TR5	R12	O			Trace output line 5
TR6	R10	O			Trace output line 4
TR7	R11	O			Trace output line 7
TR8	M11	O			Trace output line 8
TR9	M10	O			Trace output line 9
TR10	L11	O			Trace output line 10
TR11	L10	O			Trace output line 11
TR12	K10	O			Trace output line 12
TR13	K11	O			Trace output line 13
TR14	L12	O			Trace output line 14
TR15	K12	O			Trace output line 15
TRCLK	T10	O	A4		**Trace Clock for OCDS Level 2 Debug Trace Lines**[1] (located on a center ball)

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Class	Power Supply	Functions
System I/O					
$\overline{\text{TRST}}$	F23	I	A2	V_{DDP}	**JTAG Module Reset/Enable Input**[2]
TCK	E24	I	A2		**JTAG Module Clock Input**[2]
TDI	E25	I	A1		**JTAG Module Serial Data Input**
TDO	D25	O	A2		**JTAG Module Serial Data Output**
TMS	F24	I	A1		**JTAG Module State Machine Control Input**
$\overline{\text{BRKIN}}$	C26	I/O	A3		**OCDS Break Input (Alternate Output)**[2]
$\overline{\text{BRK OUT}}$	D26	I/O	A3		**OCDS Break Output (Alternate Input)**[2]
$\overline{\text{NMI}}$	A22	I	–		**Non-Maskable Interrupt Input** (input pad with input spike-filter.)
$\overline{\text{HDRST}}$	A23	I/O	A2		**Hardware Reset Input / Reset Indication Output** (open drain pad with input spike-filter.)
$\overline{\text{PORST}}$	B22	I	–		**Power-on Reset Input** (input pad with input spike-filter.)
BYPASS	A24	I	A1		**PLL Bypass Select Input** This input has to be held stable between to power-on resets. With BYPASS = 1 the spike filters in the $\overline{\text{HDRST}}$, $\overline{\text{PORST}}$, and $\overline{\text{NMI}}$ inputs are switched off.
$\overline{\text{TEST MODE}}$	B23	I	–		**Test Mode Select Input** For normal operation of the TC1796, this pin should be connected to high level. (input pad, test function only, without input spike-filter.)
TSTRES	G24	I	–		**Test Reset Input** For normal operation of the TC1796, this pin should be connected to low level. Otherwise an unpredictable reset behavior may occur. (input pad, test function only, without input spike-filter.)

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Class	Power Supply	Functions
XTAL1 **XTAL2**	G26 G25	I O	n.a.	V_{DD}	**Oscillator / PLL / Clock Generator Input / Output Pins**[2]
N.C.	A1 C22 G23 H3 AF1 AF26 AC21 AD23 AE22 AE23	–	–	–	**Not Connected** These pins are reserved for future extension and should not be connected externally.
Power Supplies					
V_{DDM}	W4	–	–	–	**ADC0/1 Analog Part Power Supply (3.3V)**
V_{SSM}	Y4	–	–	–	**ADC0/1 Analog Part Ground for V_{DDM}**
V_{DDMF}	AE9	–	–	–	**FADC Analog Part Power Supply (3.3V)**
V_{SSMF}	AF9	–	–	–	**VFADC Analog Part Ground for V_{DDAF}**
V_{DDAF}	AC9	–	–	–	**FADC Analog Part Log. Pow. Sup. (1.5V)**
V_{SSAF}	AD9	–	–	–	**FADC Analog Part Log Ground for V_{DDAF}**
V_{AREF0}	AE5	–	–	–	**ADC0 Reference Voltage**
V_{AGND0}	AF5	–	–	–	**ADC0 Reference Ground**
V_{AREF1}	AD6	–	–	–	**ADC1 Reference Voltage**
V_{AGND1}	AC6	–	–	–	**ADC1 Reference Ground**
V_{FAREF}	AF8	–	–	–	**FADC Reference Voltage**
V_{FAGND}	AE8	–	–	–	**FADC Reference Ground**
V_{DDOSC}[3]	F26	–	–	–	**Main Oscillator Power Supply (1.5V)**
V_{DDOSC3}	E26	–	–	–	**Main Oscillator Power Supply (3.3V)**
V_{SSOSC}[3]	F25	–	–	–	**Main Oscillator Ground**
V_{DDFL3}	A18 B18	–	–	–	**Power Supply for Flash (3.3V)**
$V_{DDSBRAM}$	R1	–	–	–	**Power Supply for Stand-by SRAM (1.5V)**

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Class	Power Supply	Functions
V_{DDEBU}	H23 H24 H25 H26 M23 T23 Y23 AC18 AC22	–	–	–	**EBU Power Supply (2.3 - 3.3V)**
V_{DD}	B26 C25 D9 D16 D24 E23 H4 P23 R4 V23 AB23 AC11 AC20	–	–	–	**Core Power Supply (1.5V)**
V_{DDP}	A25 B24 C23 D7 D14 D22 K4 AC16 AD16 AE16 AF16	–	–	–	**Port Power Supply (3.3V)** (also for OCDS)
V_{SS}	See Table 3	–	–	–	**Ground** 15 V_{SS} lines are located at outer balls. 47 V_{SS} lines are located at center balls.

1) In order to minimize noise coupling to the on-chip A/D converters, it is recommended to use these pins as less as possible in strong driver mode.

2) In case of a power-fail condition (one or more power supply voltages drop below the specified voltage range), an undefined output driving level may occur at these pins.

3) Not bonded externally in the BC and BD steps of TC1796. An option for bonding them in future steps and products is kept open.

Table 3 V_{SS} Balls

V_{SS} Outer Balls	V_{SS} Center Balls
A26, B25, C24, D8, D15, D23, J4, L23, R23, T4, W23, AC10, AC17, AC19, AC23	K[17:13], L[17:13], M[17:12], N[17:10], P[17:10], R[17:13], T[17:13], U[17:13]

2.5.1 Pull-Up/Pull-Down Behavior of the Pins

Table 4 List of Pull-Up/Pull-Down Reset Behavior of the Pins

Pins	$\overline{\text{PORST}}$ = 0	$\overline{\text{PORST}}$ = 1
$\overline{\text{TSTRES}}$, $\overline{\text{TDI}}$, TMS, $\overline{\text{TESTMODE}}$, $\overline{\text{BRKOUT}}$, $\overline{\text{BRKIN}}$, all GPIOs, $\overline{\text{RD}}$, RD/$\overline{\text{WR}}$, $\overline{\text{ADV}}$, $\overline{\text{BC}}$[3:0], MR/$\overline{\text{W}}$, $\overline{\text{WAIT}}$, $\overline{\text{BAA}}$, $\overline{\text{HOLD}}$, $\overline{\text{HLDA}}$, $\overline{\text{BREQ}}$, $\overline{\text{D}}$[31:0], $\overline{\text{A}}$[23,0], $\overline{\text{CS}}$[3:0], $\overline{\text{CSCOMB}}$	Weak pull-up device active	
$\overline{\text{NMI}}$, $\overline{\text{PORST}}$	Weak pull-down device active	
BYPASS, SLSO0, SLSO1, MTSR0, MRST0, SCLK0, SLSI0, TDO, BFCLKI	Weak pull-up device active	High-impedance
BFCLKO	Weak pull-up device active	Push-pull driver active
$\overline{\text{HDRST}}$	Open-drain device drives 0 (strong pull-down)	Weak pull-up device active Open-drain device active
$\overline{\text{TRST}}$, TCK	High-impedance	Weak pull-down device active

3 Functional Description

The following section gives an overview of the sub systems and the modules of the TC1796 and their connectivity.

3.1 System Architecture and On-Chip Bus Systems

The TC1796 has four independent on-chip buses (see also TC1796 block diagram in **Figure 1**):

- Program Local Memory Bus (PLMB)
- Data Local Memory Bus (DLMB)
- System Peripheral Bus (SPB)
- Remote Peripheral Bus (RPB)

The two LMB Buses (Program Local Memory Bus PLMB and Data Local Memory Bus DLMB) connect the TriCore CPU to its local resources for data and instruction fetches. The PLMB/DLMB Buses are synchronous and pipelined buses with variable block size transfer support. The protocol supports 8-, 16-, 32-, and 64-bit single transactions and variable length 64-bit block transfers.

The System Peripheral Bus (SPB) is accessible by the CPU via the LFI Bridge. The LFI Bridge is a bi-directional bus bridge between the DLMB and the SPB. It supports all transactions types of both buses, DLMB Bus and FPI Bus. It handles address translation and transaction type translation between the two buses. The LFI Bridge further supports the pipelining of both connected buses. Therefore, no additional delay is created except for bus protocol conversions.

The Remote Peripheral Bus (RPB) connects the peripherals with high data rates (SSC, ADC, FADC) with the Dual-port memory (DPRAM) in the DMI, relieving the SPB and the PLMB/DLMB Buses from these data transfers. The RPB is controlled by a bus switch which is located in the DMA controller.

The two LMB Buses are running at CPU clock speed (clock rate of f_{CPU}) while SPB and RPB are running at system clock speed (clock rate of f_{SYS}). Note that f_{SYS} can be equal to f_{CPU} or half the f_{CPU} frequency.

3.2 On-Chip Memories

As shown in the TC1796 block diagram on **Page 10**, some of the TC1796 units provide on-chip memories that are used as program or data memory.

- Program memory in PMU and PMI
  - 2 Mbyte on-chip Program Flash (PFLASH)
  - 16 Kbyte Boot ROM (BROM)
  - 48 Kbyte Scratch-Pad RAM (SPRAM)
  - 16 Kbyte Instruction Cache (ICACHE)
- Data memory in DMU, PMU and DMI
  - 56 Kbyte Local Data RAM (LDRAM)
  - 8 Kbyte Dual-port RAM (DPRAM)
  - 64 Kbyte Data Memory (SRAM)
  - 16 Kbyte data memory (SBRAM) for standby operation during power-down
  - 128 Kbyte on-chip Data Flash (DFLASH)
- Memory of the PCP2
  - 32 Kbyte Code Memory (CMEM)
  - 16 Kbyte Parameter Memory (PRAM)
- On-chip SRAMs with parity error detection

Features of the Program Flash

- 2 Mbyte on-chip program Flash memory
- Usable for instruction code execution or constant data storage
- 256-byte wide program interface
  - 256 bytes are programmed into PFLASH page in one step/command
- 256-bit read interface
  - Transfer from PFLASH to CPU/PMI by four 64-bit single-cycle burst transfers
- Dynamic correction of single-bit errors during read access
- Detection of double bit errors
- Fixed sector architecture
  - Eight 16 Kbyte, one 128 Kbyte, one 256 Kbyte, and three 512 Kbyte sectors
  - Each sector separately erasable
  - Each sector separately write-protectable
- Configurable read protection for complete PFLASH with sophisticated read access supervision, combined with write protection for complete PFLASH (protection against “Trojan horse” software)
- Configurable write protection for each sector
  - Each sector separately write-protectable
  - With capability to be re-programmed
  - With capability to be locked forever (OTP)
- Password mechanism for temporarily disable write or read protection
- On-chip programming voltage generation
- PFLASH is delivered in erased state (read all zeros)

- JEDEC standard based command sequences for PFLASH control
  - Write state machine controls programming and erase operations
  - Status and error reporting by status flags and interrupt
- Margin check for detection of problematic PFLASH bits

Features of the Data Flash

- 128 Kbyte on-chip data Flash memory, organized in two 64 Kbyte banks
- Usable for data storage with EEPROM functionality
- 128 Byte program interface
  - 128 bytes are programmed into one DFLASH page by one step/command
- 64-bit read interface (no burst transfers)
- Dynamic correction of single-bit errors during read access
- Detection of double bit errors
- Fixed sector architecture
  - Two 64 Kbyte banks/sectors
  - Each sector separately erasable
- Configurable read protection (combined with write protection) for complete DFLASH together with PFLASH read protection
- Password mechanism to temporarily disable write and read protection
- Erasing/programming of one bank possible while reading data from the other bank
- Programming of one bank possible while erasing the other bank
- On-chip generation of programming voltage
- DFLASH is delivered in erased state (read all zeros)
- JEDEC-standard based command sequences for DFLASH control
  - Write state machine controls programming and erase operations
  - Status and error reporting by status flags and interrupt
- Margin check for detection of problematic DFLASH bits

3.3 Architectural Address Map

Table 5 shows the overall architectural address map as defined for the TriCore and implemented in TC1796.

Table 5 TC1796 Architectural Address Map

Seg-ment	Contents	Size	Description
0-7	Global	8 × 256 Mbyte	Reserved (MMU space), cached
8	Global Memory	256 Mbyte	EBU (246 Mbyte), PMU with PFLASH, DFLASH, BROM, memory reserved for Emulation, cached
9	Global Memory	256 Mbyte	FPI space; cached
10	Global Memory	256 Mbyte	EBU (246 Mbyte), PMU with PFLASH, DFLASH, BROM, memory reserved for Emulation, non-cached
11	Global Memory	256 Mbyte	FPI space; non-cached
12	Local LMB Memory	256 Mbyte	DMU, bottom 4 Mbyte visible from FPI Bus in segment 14, cached
13	DMI	64 Mbyte	Local Data Memory RAM, non-cached
	PMI	64 Mbyte	Local Code Memory RAM, non-cached
	EXTPER	96 Mbyte	External Peripheral Space, non-cached
	EXTEMU	16 Mbyte	External Emulator Range, non-cached
	BOOTROM	16 Mbyte	Boot ROM space, BROM mirror; non-cached
14	EXTPER	128 Mbyte	External Peripheral Space non-speculative, no execution, non-cached
	CPU[0 ..15] image region	16 × 8 Mbyte	Non-speculative, no execution, non-cached
15	LMBPER CSFRs INTPER	256 Mbyte	CSFRs of CPUs[0 ..15]; LMB & Internal Peripheral Space; non-speculative, no execution, non-cached

3.4 Memory Protection System

The TC1796 memory protection system specifies the addressable range and read/write permissions of memory segments available to the currently executing task. The memory protection system controls the position and range of addressable segments in memory. It also controls the kinds of read and write operations allowed within addressable memory segments. Any illegal memory access is detected by the memory protection hardware, which then invokes the appropriate Trap Service Routine (TSR) to handle the error. Thus, the memory protection system protects critical system functions against both software and hardware errors. The memory protection hardware can also generate signals to the Debug Unit to facilitate tracing illegal memory accesses.

There are two Memory Protection Register Sets in the TC1796, numbered 0 and 1, which specify memory protection ranges and permissions for code and data. The PSW.PRS bit field determines which of these is the set currently in use by the CPU. Because the TC1796 uses a Harvard-style memory architecture, each Memory Protection Register Set is broken down into a Data Protection Register Set and a Code Protection Register Set. Each Data Protection Register Set can specify up to four address ranges to receive particular protection modes. Each Code Protection Register Set can specify up to two address ranges to receive particular protection modes.

Each of the Data Protection Register Sets and Code Protection Register Sets determines the range and protection modes for a separate memory area. Each contains register pairs which determine the address range (the Data Segment Protection Registers and Code Segment Protection Registers) and one register (Data Protection Mode Register) which determines the memory access modes which apply to the specified range.

3.5 External Bus Unit

The External Bus Unit (EBU) of the TC1796 is the units that controls the transactions between external memories or peripheral units with the internal memories and peripheral units. The EBU is a part of the PMU and communicates with CPU and PMI via the Program Local Memory Bus. This configuration allows to get fast access times especially when using external burst FLASH memory devices.

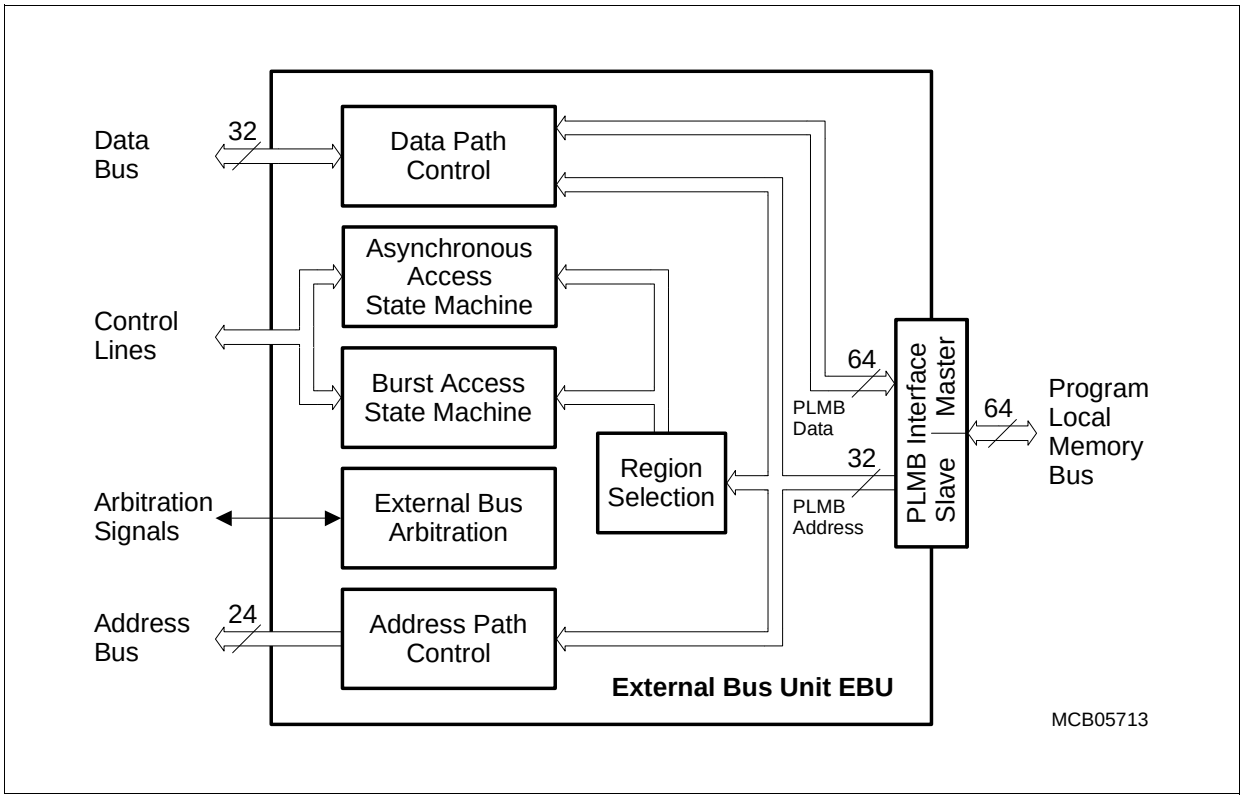


Figure 4 EBU Block Diagram

The following features are supported by the EBU:

- 64-bit internal Program Local Memory Bus (PLMB) interface
- 32-bit external demultiplexed bus interface
  - Asynchronous read/write accesses support Intel-style and Motorola-style interface signals
  - Synchronous burst FLASH memory read
  - Five programmable regions associated each to one chip select output
  - Flexibly programmable access parameters for each chip select region
  - Little-endian and Big-endian support
  - Programmable wait state control
- Scalable external bus frequency
  - Derived from PLMB frequency (f_{CPU}) divided by 1, 2, 3, or 4
  - Max. 75 MHz

- Data buffering supported
  - Code prefetch buffer
  - Read/write buffer
- External bus arbitration control capability for the EBU bus
- Automatic self-configuration on boot from external memory

3.6 Peripheral Control Processor

The Peripheral Control Processor (PCP2) in the TC1796 performs tasks that would normally be performed by the combination of a DMA controller and its supporting CPU interrupt service routines in a traditional computer system. It could easily be considered as the host processor's first line of defence as an interrupt-handling engine. The PCP2 can off-load the CPU from having to service time-critical interrupts. This provides many benefits, including:

- Avoiding large interrupt-driven task context-switching latencies in the host processor
- Reducing the cost of interrupts in terms of processor register and memory overhead
- Improving the responsiveness of interrupt service routines to data-capture and data-transfer operations
- Easing the implementation of multitasking operating systems.

The PCP2 has an architecture that efficiently supports DMA-type transactions to and from arbitrary devices and memory addresses within the TC1796 and also has reasonable stand-alone computational capabilities.

The PCP2 in the TC1796 contains an improved version of the TC1775's PCP with the following enhancements:

- Optimized context switching
- Support for nested interrupts
- Enhanced instruction set
- Enhanced instruction execution speed
- Enhanced interrupt queueing

The PCP2 is made up of several modular blocks as follows (see **Figure 5**):

- PCP2 Processor Core
- Code Memory (CMEM)
- Parameter Memory (PRAM)
- PCP2 Interrupt Control Unit (PICU)
- PCP2 Service Request Nodes (PSRN)
- System bus interface to the Flexible Peripheral Interface (FPI Bus)

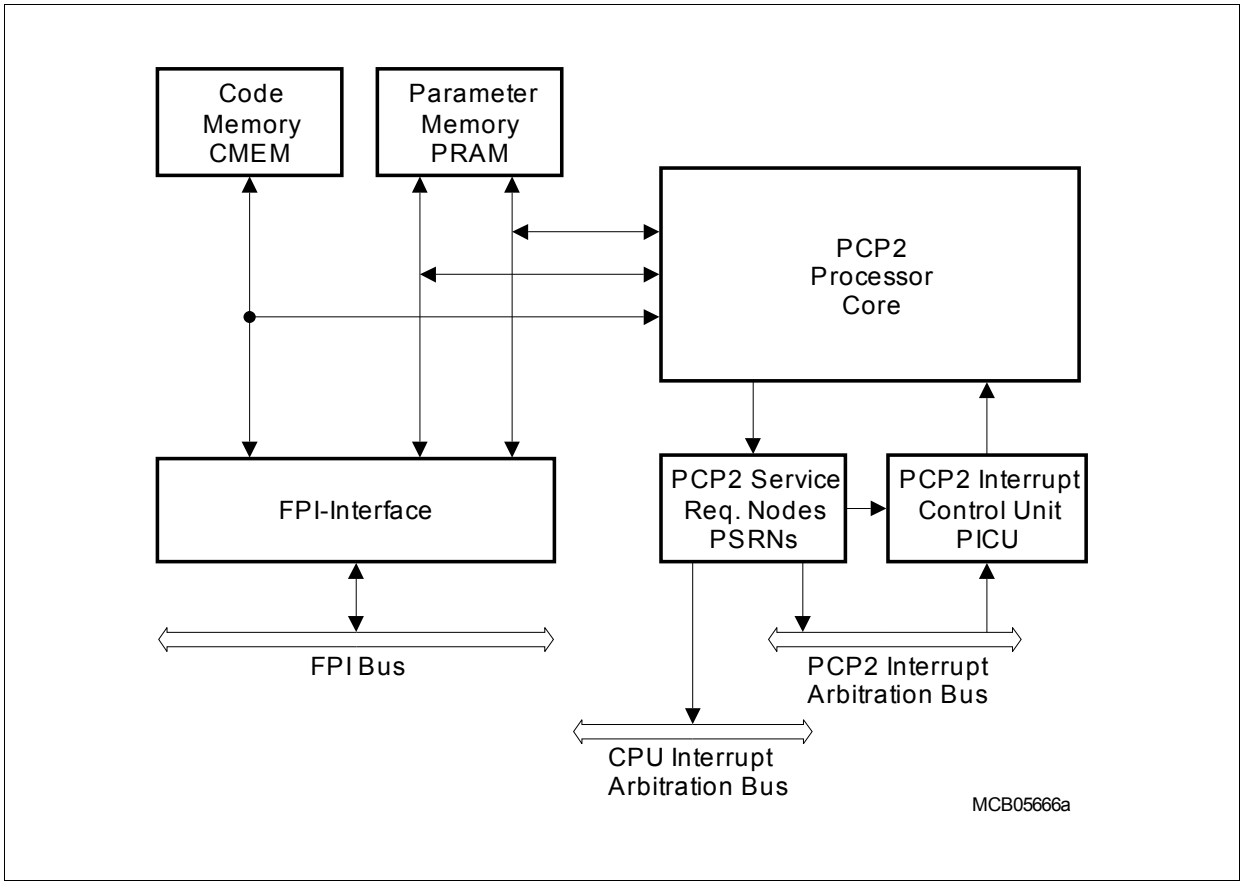


Figure 5 PCP2 Block Diagram

Table 6 PCP2 Instruction Set Overview

Instruction Group	Description
DMA primitives	Efficient DMA channel implementation
Load/Store	Transfer data between PRAM or FPI memory and the general purpose registers, as well as move or exchange values between registers
Arithmetic	Add, subtract, compare and complement
Divide/Multiply	Divide and multiply
Logical	And, Or, Exclusive Or, Negate
Shift	Shift right or left, rotate right or left, prioritize
Bit Manipulation	Set, clear, insert and test bits
Flow Control	Jump conditionally, jump long, exit
Miscellaneous	No operation, Debug

3.7 DMA Controller and Memory Checker

The Direct Memory Access (DMA) Controller of the TC1796 transfers data from data source locations to data destination locations without intervention of the CPU or other on-chip devices. One data move operation is controlled by one DMA channel. Sixteen DMA channels are provided in two independent DMA Sub-Blocks with eight DMA channels each. The Bus Switch provides the connection of two DMA Sub-Blocks to the two FPI Bus interfaces and an MLI bus interface. In the TC1796, the FPI Bus interfaces are connected to System Peripheral Bus and the Remote Peripheral Bus. The third specific bus interface provides a connection to Micro Link Interface modules (two MLI modules in the TC1796) and other DMA-related devices (Memory Checker module in the TC1796). **Figure 6** shows the implementation details and interconnections of the DMA module.

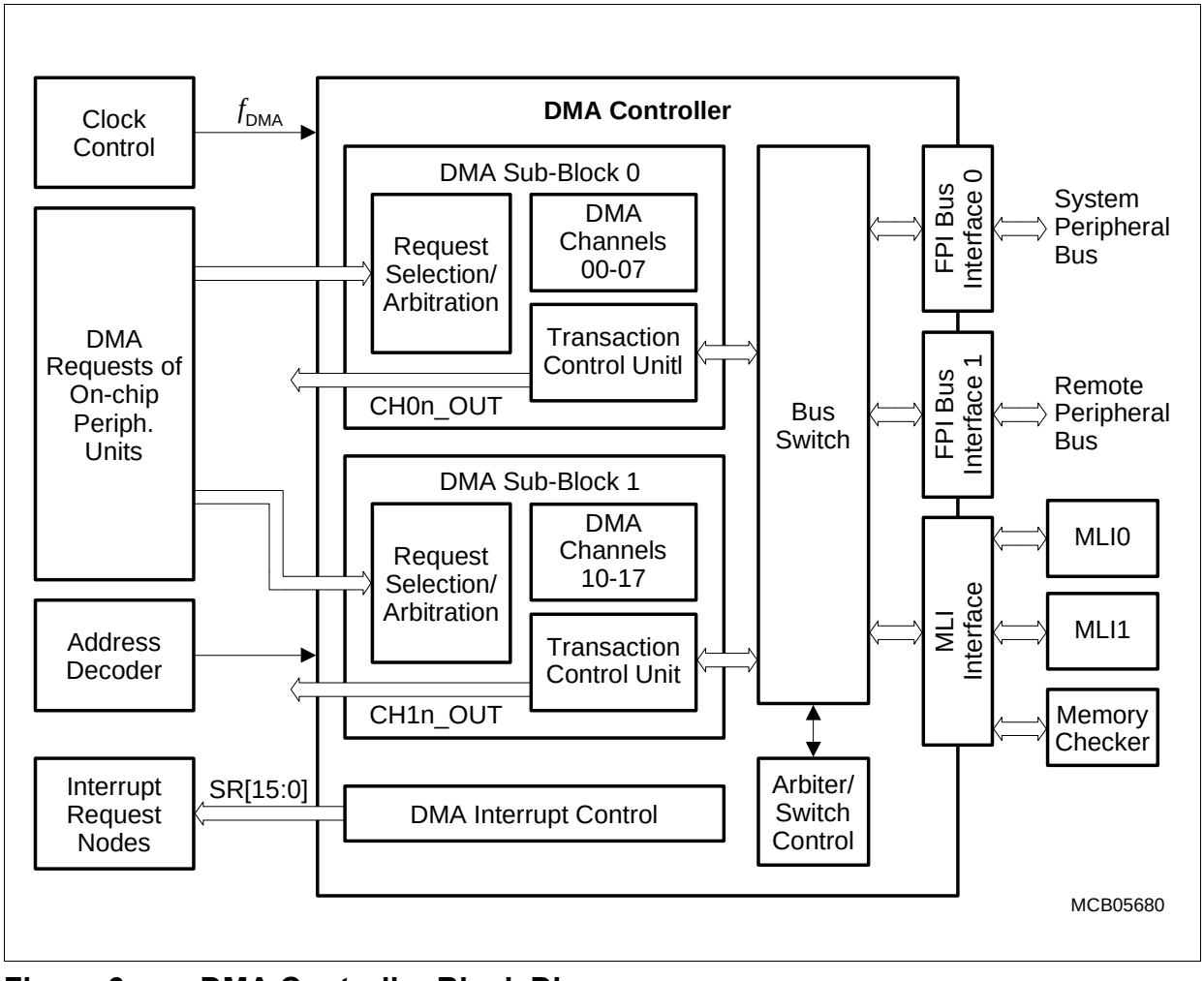


Figure 6 DMA Controller Block Diagram

Features

- 16 independent DMA channels
  - 8 DMA channels in each DMA Sub-Block
  - Up to 8 selectable request inputs per DMA channel
  - 2-level programmable priority of DMA channels within a DMA Sub-Block
  - Software and hardware DMA request
  - Hardware requests by selected on-chip peripherals and external inputs
- Programmable priority of the DMA Sub-Blocks on the bus interfaces
- Buffer capability for move actions on the buses (at least 1 move per bus is buffered).
- Individually programmable operation modes for each DMA channel
  - Single mode: stops and disables DMA channel after a predefined number of DMA transfers
  - Continuous mode: DMA channel remains enabled after a predefined number of DMA transfers; DMA transaction can be repeated.
  - Programmable address modification
- Full 32-bit addressing capability of each DMA channel
  - 4 GByte address range
  - Support of circular buffer addressing mode
- Programmable data width of DMA transfer/transaction: 8-bit, 16-bit, or 32-bit
- Micro Link bus interface support
- Register set for each DMA channel
  - Source and destination address register
  - Channel control and status register
  - Transfer count register
- Flexible interrupt generation (the service request node logic for the MLI channels is also implemented in the DMA module)
- All buses connected to the DMA module must work at the same frequency.
- Read/write requests of the System Bus Side to the Remote Peripherals are bridged to the Remote Peripheral Bus (only the DMA is master on the RPB)

Memory Checker

The Memory Checker Module (MEMCHK) makes it possible to check the data consistency of memories. Any SPB bus master may access the memory checker. Preferable the DMA controller does it as described hereafter. It uses 8-bit, 16-bit, or 32-bit DMA moves to read from the selected address area and to write the value read in a memory checker input register. With each write operation to the memory checker input register, a polynomial checksum calculation is triggered and the result of the calculation is stored in the memory checker result register.

The memory checker uses the standard Ethernet polynomial, which is given by:

$G^{32} = x^{32}+ x^{26}+ x^{23}+ x^{22}+ x^{16}+ x^{12}+ x^{11}+ x^{10}+ x^{8}+ x^{7}+ x^{5}+ x^{4}+ x^{2}+ x +1$

Note: Although the polynomial above is used for generation, the generation algorithm differs from the one that is used by the Ethernet protocol.

3.8 Interrupt System

The TC1796 interrupt system provides a flexible and time-efficient means for processing interrupts. An interrupt request can be serviced either by the CPU or by the Peripheral Control Processor (PCP). These units are called “Service Providers”. Interrupt requests are called “Service Requests” rather than “Interrupt Requests” in this document because they can be serviced by either of the Service Providers.

Each peripheral in the TC1796 can generate service requests. Additionally, the Bus Control Units, the Debug Unit, the PCP, and even the CPU itself can generate service requests to either of the two Service Providers.

As shown in **Figure 7**, each TC1796 unit that can generate service requests is connected to one or more Service Request Nodes (SRN). Each SRN contains a Service Request Control Register. Two arbitration buses connect the SRNs with two Interrupt Control Units, which handle interrupt arbitration among competing interrupt service requests, as follows:

- The Interrupt Control Unit (ICU) arbitrates service requests for the CPU and administers the CPU Interrupt Arbitration Bus.
- The Peripheral Interrupt Control Unit (PICU) arbitrates service requests for the PCP2 and administers the PCP2 Interrupt Arbitration Bus.

The PCP2 can make service requests directly to itself (via the PICU), or it can make service requests to the CPU. The Debug Unit can generate service requests to the PCP2 or the CPU. The CPU can make service requests directly to itself (via the ICU), or it can make service requests to the PCP. The CPU Service Request Nodes are activated through software.

Depending on the selected system clock frequency f_{SYS}, the number of f_{SYS} clock cycles per arbitration cycle must be selected as follows:

- $f_{SYS} < 60MHz$: ICR.CONECYC = 1 and PCP_ICR.CONECYC = 1
- $f_{SYS} > 60MHz$: ICR.CONECYC = 0 and PCP_ICR.CONECYC = 0

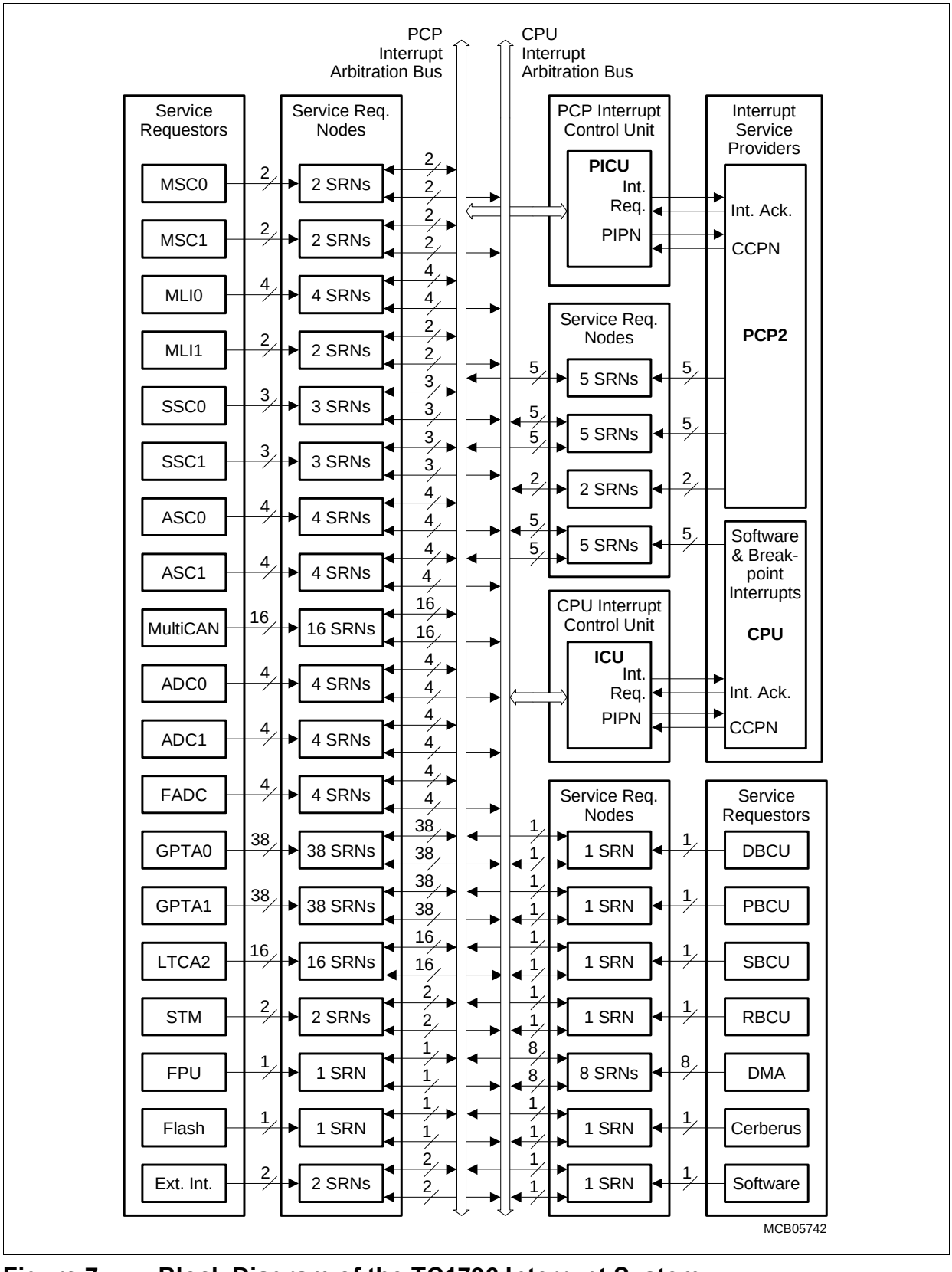


Figure 7 Block Diagram of the TC1796 Interrupt System

3.9 Asynchronous/Synchronous Serial Interfaces (ASC0, ASC1)

Figure 8 shows a global view of the functional blocks and interfaces of the two Asynchronous/Synchronous Serial Interfaces ASC0 and ASC1.

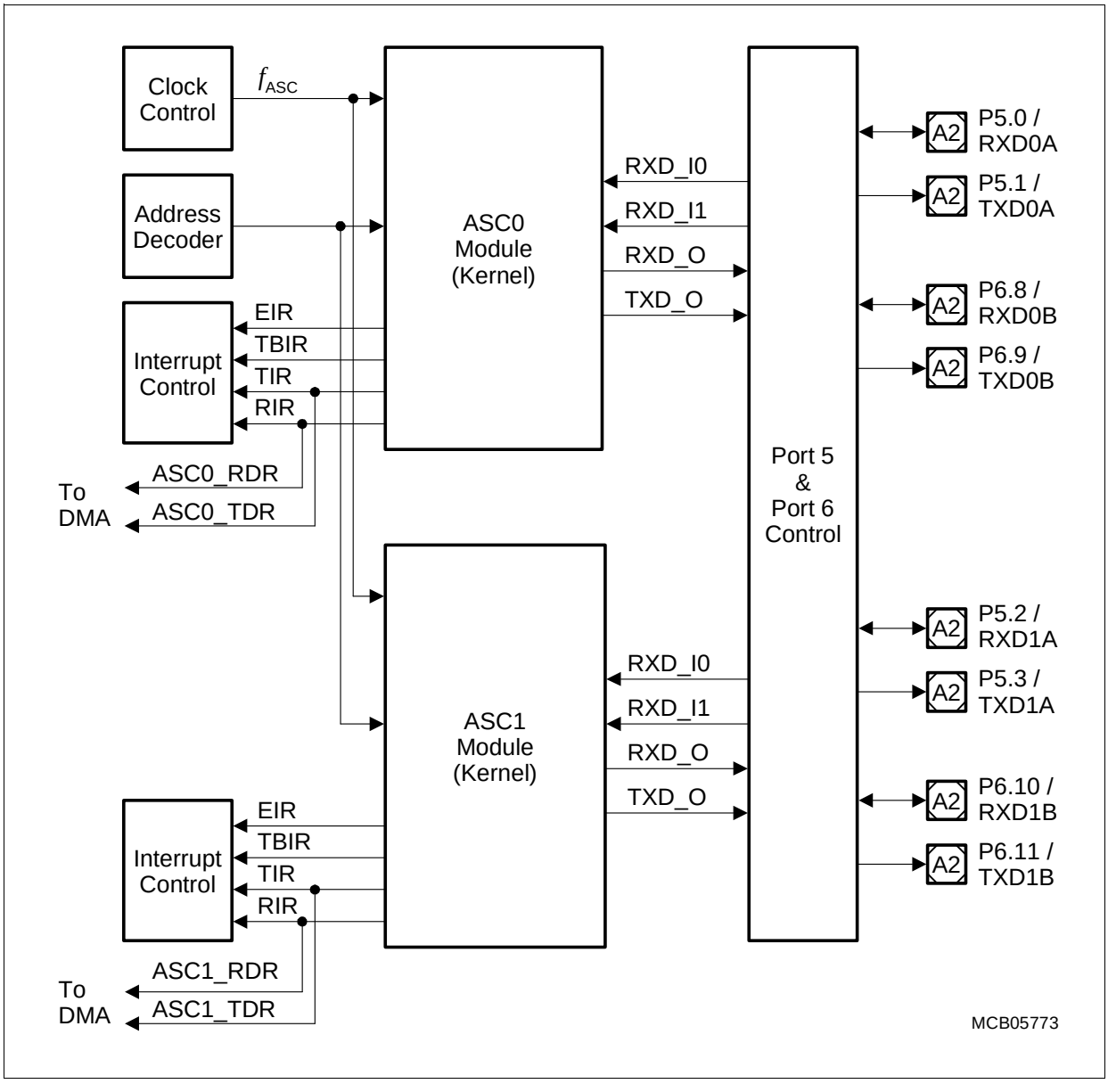


Figure 8 Block Diagram of the ASC Interfaces

The Asynchronous/Synchronous Serial Interfaces provide serial communication between the TC1796 and other microcontrollers, microprocessors, or external peripherals.

The ASC supports full-duplex asynchronous communication and half-duplex synchronous communication. In Synchronous Mode, data is transmitted or received synchronous to a shift clock which is generated by the ASC internally. In Asynchronous

Mode, 8-bit or 9-bit data transfer, parity generation, and the number of stop bits can be selected. Parity, framing, and overrun error detection are provided to increase the reliability of data transfers. Transmission and reception of data are double-buffered. For multiprocessor communication, a mechanism is included to distinguish address bytes from data bytes. Testing is supported by a loop-back option. A 13-bit baud rate generator provides the ASC with a separate serial clock signal which can be very accurately adjusted by a prescaler implemented as a fractional divider.

Each ASC module, ASC0 and ASC1, communicates with the external world via two I/O lines. The RXD line is the receive data input signal (in Synchronous Mode also output). TXD is the transmit output signal. In the TC1796, the two I/O lines of each ASC can be alternatively switched to different pairs of GPIO lines.

Clock control, address decoding, and interrupt service request control are managed outside the ASC module kernel.

Features

- Full-duplex asynchronous operating modes
  - 8-bit or 9-bit data frames, LSB first
  - Parity bit generation/checking
  - One or two stop bits
  - Baud rate from 4.69 Mbit/s to 1.12 Bit/s (@ 75 MHz clock)
  - Multiprocessor mode for automatic address/data byte detection
  - Loop-back capability
- Half-duplex 8-bit synchronous operating mode
  - Baud rate from 9.38 Mbit/s to 763 Bit/s (@ 75 MHz clock)
- Double buffered transmitter/receiver
- Interrupt generation
  - On a transmit buffer empty condition
  - On a transmit last bit of a frame condition
  - On a receive buffer full condition
  - On an error condition (frame, parity, overrun error)

3.10 High-Speed Synchronous Serial Interfaces (SSC0, SSC1)

Figure 9 shows a global view of the functional blocks and interfaces of the two High-Speed Synchronous Serial interfaces SSC0 and SSC1.

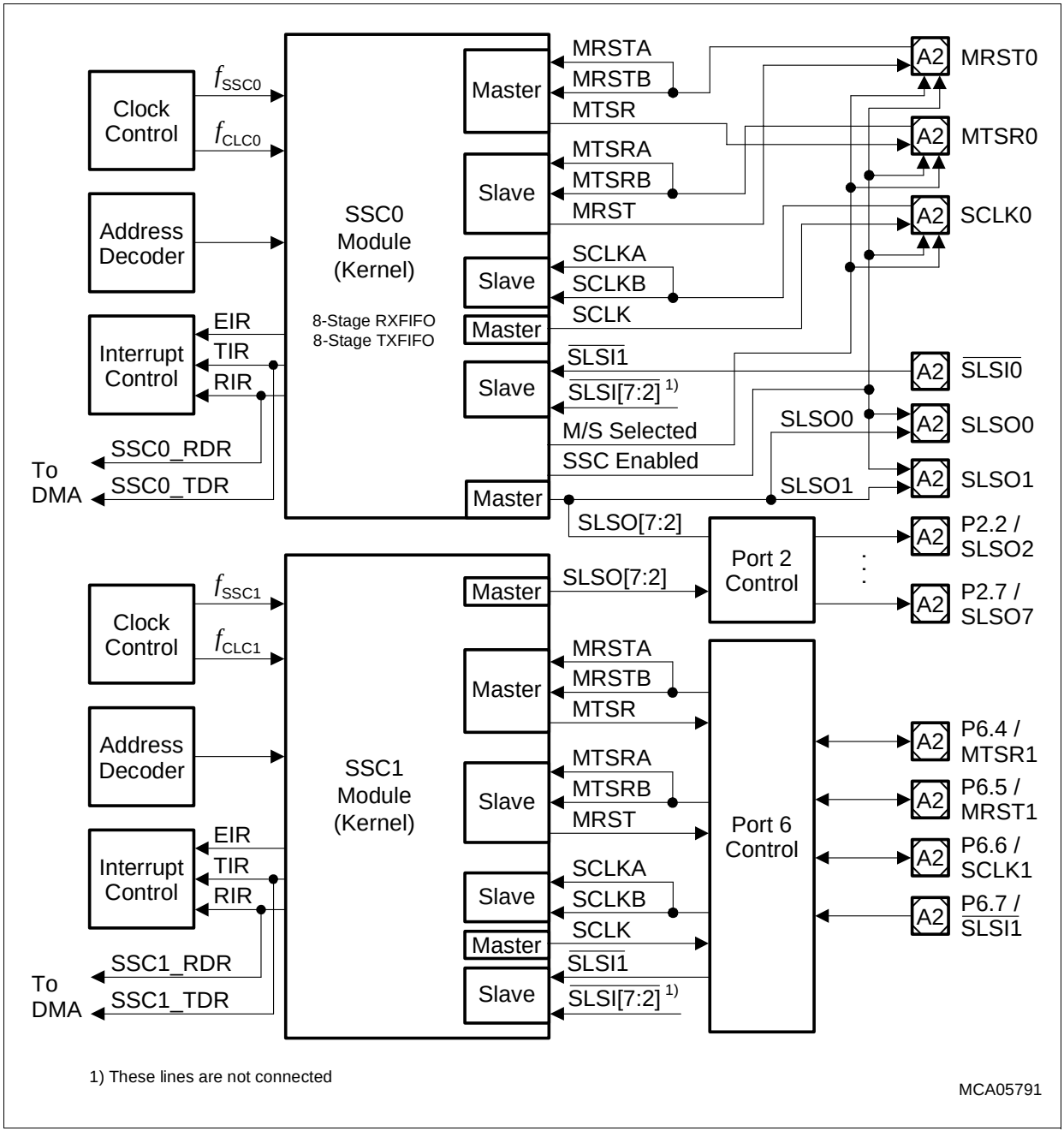


Figure 9 Block Diagram of the SSC Interfaces

The SSC allows full-duplex and half-duplex serial synchronous communication up to 37.5 Mbit/s (@ 75 MHz module clock) with Receive and Transmit FIFO support. (FIFO only in SSC0). The serial clock signal can be generated by the SSC itself (Master Mode)

or can be received from an external master (Slave Mode). Data width, shift direction, clock polarity and phase are programmable. This allows communication with SPI-compatible devices. Transmission and reception of data is double-buffered. A shift clock generator provides the SSC with a separate serial clock signal. One slave select input is available for Slave Mode operation. Eight programmable slave select outputs (chip selects) are supported in Master Mode. The I/O lines of the SSC0 module are connected to dedicated device pins while the SSC1 module I/O lines are wired with general purpose I/O port lines.

Features

- Master and Slave Mode operation
  - Full-duplex or half-duplex operation
  - Automatic pad control possible
- Flexible data format
  - Programmable number of data bits: 2 to 16 bits
  - Programmable shift direction: LSB or MSB shift first
  - Programmable clock polarity: Idle low or high state for the shift clock
  - Programmable clock/data phase: data shift with leading or trailing edge of the shift clock
- Baud rate generation from 37.5 Mbit/s to 572.2 Bit/s (@ 75 MHz module clock)
- Interrupt generation
  - On a transmitter empty condition
  - On a receiver full condition
  - On an error condition (receive, phase, baud rate, transmit error)
- Flexible SSC pin configuration
- One slave select input $\overline{\text{SLSI}}$ in slave mode
- Eight programmable slave select outputs SLSO in Master Mode
  - Automatic SLSO generation with programmable timing
  - Programmable active level and enable control
- SSC0 with 8-stage receive FIFO (RXFIFO) and 8-stage transmit FIFO (TXFIFO)
  - Independent control of RXFIFO and TXFIFO
  - 2- to 16-bit FIFO data width
  - Programmable receive/transmit interrupt trigger level
  - Receive and Transmit FIFO filling level indication
  - Overrun error generation
  - Underflow error generation

3.11 Micro Second Bus Interfaces (MSC0, MSC1)

The Micro Second Channel (MSC) interfaces provides a serial communication link typically used to connect power switches or other peripheral devices. The serial communication link is build up by a fast synchronous downstream channel and a slow asynchronous upstream channel. **Figure 10** shows a global view the interface signals of the MSC interface.

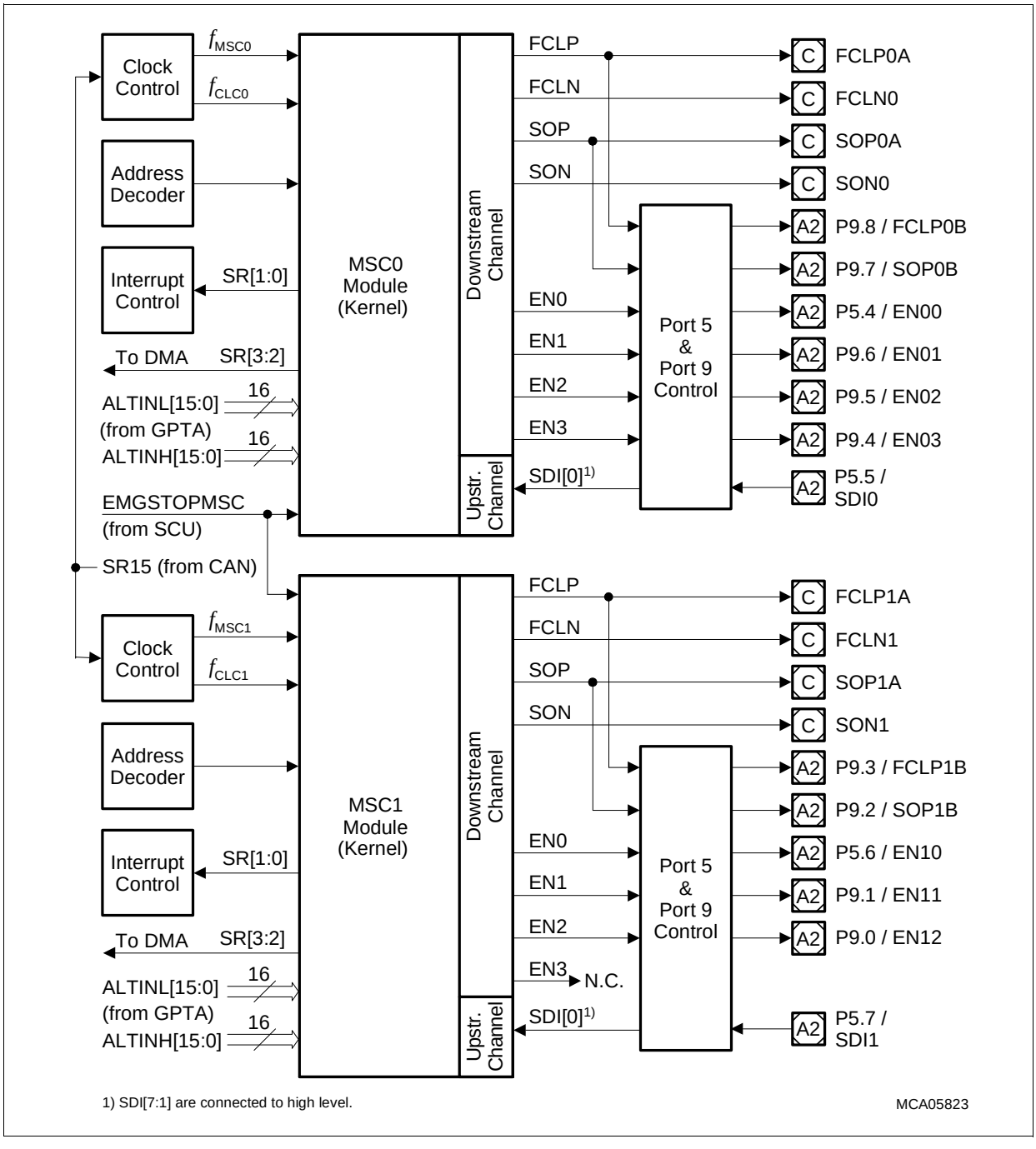


Figure 10 Block Diagram of the MSC Interfaces

The downstream and upstream channels of the MSC module communicate with the external world via nine I/O lines. Eight output lines are required for the serial communication of the downstream channel (clock, data, and enable signals). One out of eight input lines SDI[7:0] is used as serial data input signal for the upstream channel. The source of the serial data to be transmitted by the downstream channel can be MSC register contents or data that is provided at the ALTINL/ALTINH input lines. These input lines are typically connected to other on-chip peripheral units (for example with a timer unit like the GPTA). An emergency stop input signal allows to set bits of the serial data stream to dedicated values in emergency case.

Clock control, address decoding, and interrupt service request control are managed outside the MSC module kernel. Service request outputs are able to trigger an interrupt or a DMA request.

Features

- Fast synchronous serial interface to connect power switches in particular, or other peripheral devices via serial buses
- High-speed synchronous serial transmission on downstream channel
  - Maximum serial output clock frequency: $f_{FCL} = f_{MSC}/2$ (= 37.5 Mbit/s @ 75 MHz module clock)
  - Fractional clock divider for precise frequency control of serial clock f_{MSC}
  - Command, data, and passive frame types
  - Start of serial frame: Software-controlled, timer-controlled, or free-running
  - Programmable upstream data frame length (16 or 12 bits)
  - Transmission with or without SEL bit
  - Flexible chip select generation indicates status during serial frame transmission
  - Emergency stop without CPU intervention
- Low-speed asynchronous serial reception on upstream channel
  - Baud rate: f_{MSC} divided by 8, 16, 32, 64, 128, 256, or 512
  - Standard asynchronous serial frames
  - Parity error checker
  - 8-to-1 input multiplexer for SDI lines
  - Built-in spike filter on SDI lines

3.12 MultiCAN Controller (CAN)

Figure 11 shows a global view of the MultiCAN module with its functional blocks and interfaces.

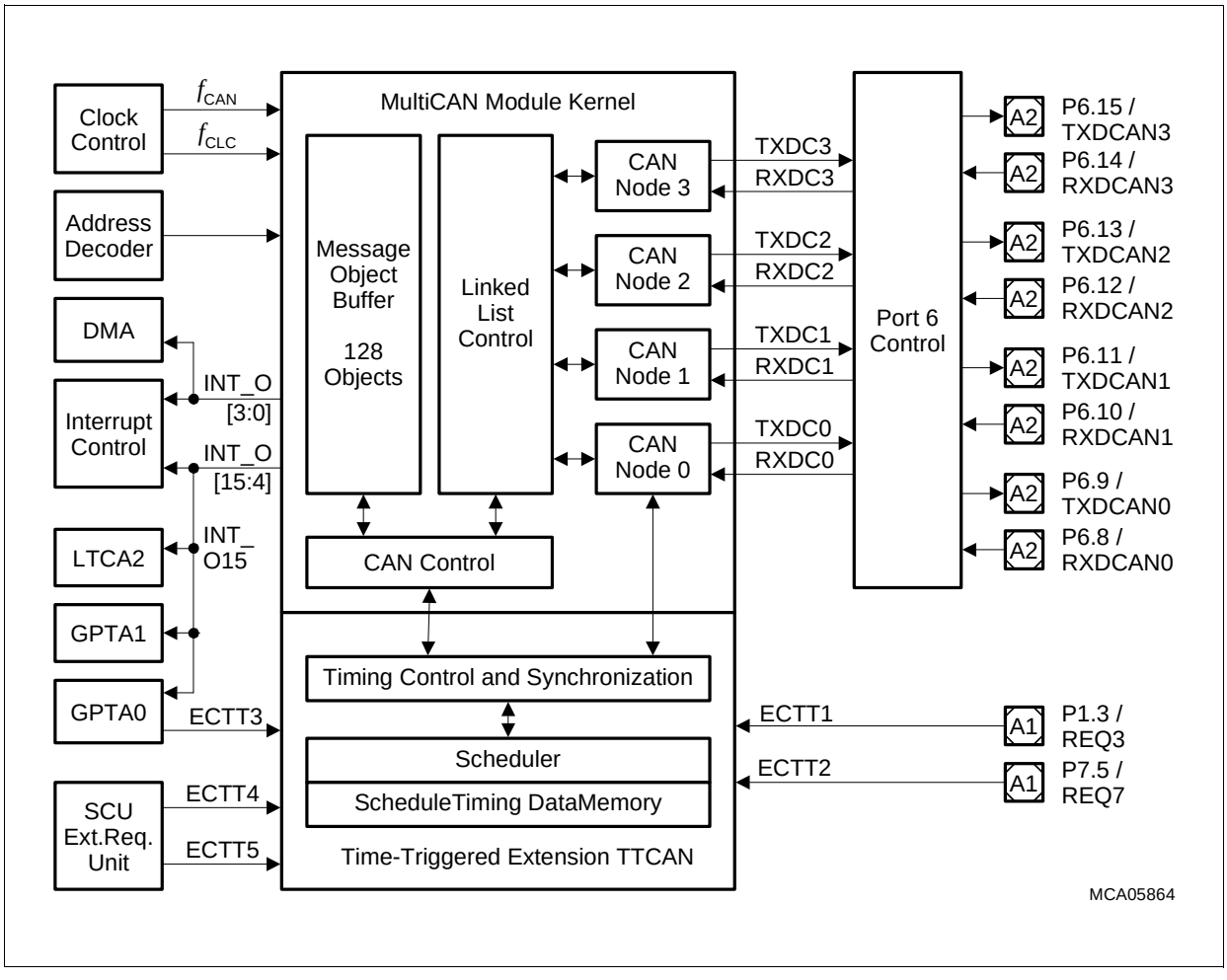


Figure 11 Block Diagram of MultiCAN Module with Time-Triggered Extension

The MultiCAN module contains four independently operating CAN nodes with Full-CAN functionality that are able to exchange Data and Remote Frames via a gateway function. Transmission and reception of CAN frames is handled in accordance with CAN specification V2.0 B (active). Each CAN node can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers.

All four CAN nodes share a common set of message objects. Each message object can be individually allocated to one of the CAN nodes. Besides serving as a storage container for incoming and outgoing frames, message objects can be combined to build gateways between the CAN nodes or to setup a FIFO buffer.

The message objects are organized in double-chained linked lists, where each CAN node has it's own list of message objects. A CAN node stores frames only into message

objects that are allocated to the message object list of the CAN node, and it transmits only messages belonging to this message object list. A powerful, command-driven list controller performs all message object list operations.

MultiCAN Features

- CAN functionality conforms to CAN specification V2.0 B active for each CAN node (compliant to ISO 11898)
- Four independent CAN nodes
- 128 independent message objects (shared by the CAN nodes)
- Dedicated control registers for each CAN node
- Data transfer rate up to 1Mbit/s, individually programmable for each node
- Flexible and powerful message transfer control and error handling capabilities
- Full-CAN functionality: message objects can be individually
  - Assigned to one of the four CAN nodes
  - Configured as transmit or receive object
  - Configured as message buffer with FIFO algorithm
  - Configured to handle frames with 11-bit or 29-bit identifiers
  - Provided with programmable acceptance mask register for filtering
  - Monitored via a frame counter
  - Configured for Remote Monitoring Mode
- Automatic Gateway Mode support
- 16 individually programmable interrupt nodes
- Analyzer mode for CAN bus monitoring

Time-Triggered Extension (TTCAN)

In addition to the event-driven CAN functionality, a deterministic behavior can be achieved for CAN node 0 by an extension module that supports time-triggered CAN (TTCAN) functionality. The TTCAN protocol is compliant with the confirmed standardization proposal for ISO 11898-4 and fully conforms to the existing CAN protocol.

The time-triggered functionality is added as higher-layer extension (session layer) to the CAN protocol in order to be able to operate in safety critical applications. The new features allow a deterministic behavior of a CAN network and the synchronization of networks. A global time information is available. The time-triggered extension is based on a scheduler mechanism with a timing control unit and a dedicated timing data part.

TTCAN Features

- Full support of basic cycle and system matrix functionality
- Support of reference messages level 1 and level 2
- Usable as time master
- Arbitration windows supported in time-triggered mode
- Global time information available
- CAN node 0 can be configured either for event-driven or for time-triggered mode
- Built-in scheduler mechanism and a timing synchronization unit
- Write protection for scheduler timing data memory
- Module-external CAN time trigger inputs (ECTTx lines) can be used as transmit trigger for a reference message
- Timing-related interrupt functionality
- Parity protection for scheduler memory

3.13 Micro Link Serial Bus Interface (MLI0, MLI1)

The Micro Link Interface (MLI) is a fast synchronous serial interface that allows to exchange data between microcontrollers of the 32-bit AUDO microcontroller family without intervention of a CPU or other bus masters. **Figure 12** shows how two microcontrollers are typically connected together via their MLI interfaces. The MLI operates in both microcontrollers as a bus master on the system bus.

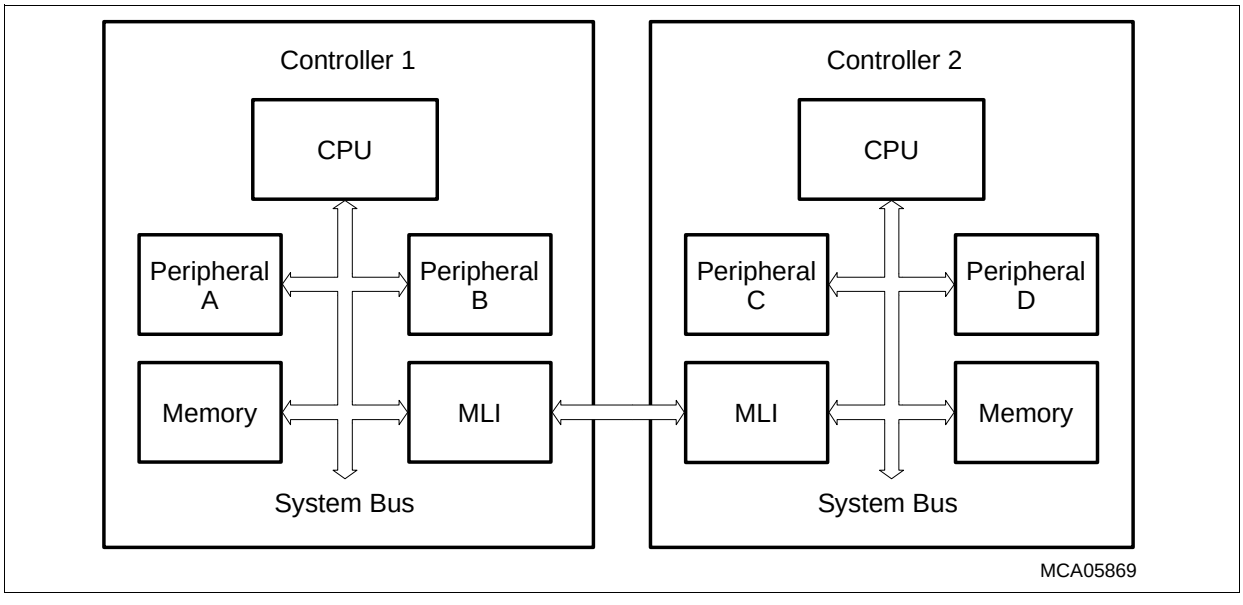


Figure 12 Typical Micro Link Interface Connection

Features

- Synchronous serial communication between MLI transmitters and MLI receivers located on the same or on different microcontroller devices
- Automatic data transfer/request transactions between local/remote controller
- Fully transparent read/write access supported (= remote programming)
- Complete address range of remote controller available
- Specific frame protocol to transfer commands, addresses and data
- Error control by parity bit
- 32-bit, 16-bit, and 8-bit data transfers
- Programmable baud rate:
  - MLI transmitter baud rate: max. $f_{MLI}/2$ (= 37.5 Mbit/s @ 75 MHz module clock)
  - MLI receiver baud rate: max. f_{MLI}
- Multiple remote (slave) controllers supported

MLI transmitter and MLI receiver communicate with other off-chip MLI receivers and MLI transmitters via a 4-line serial I/O bus each. Several I/O lines of these I/O buses are available outside the MLI module kernel as four-line output or input buses.

Figure 13 shows the functional blocks of the two MLI modules with its interfaces.

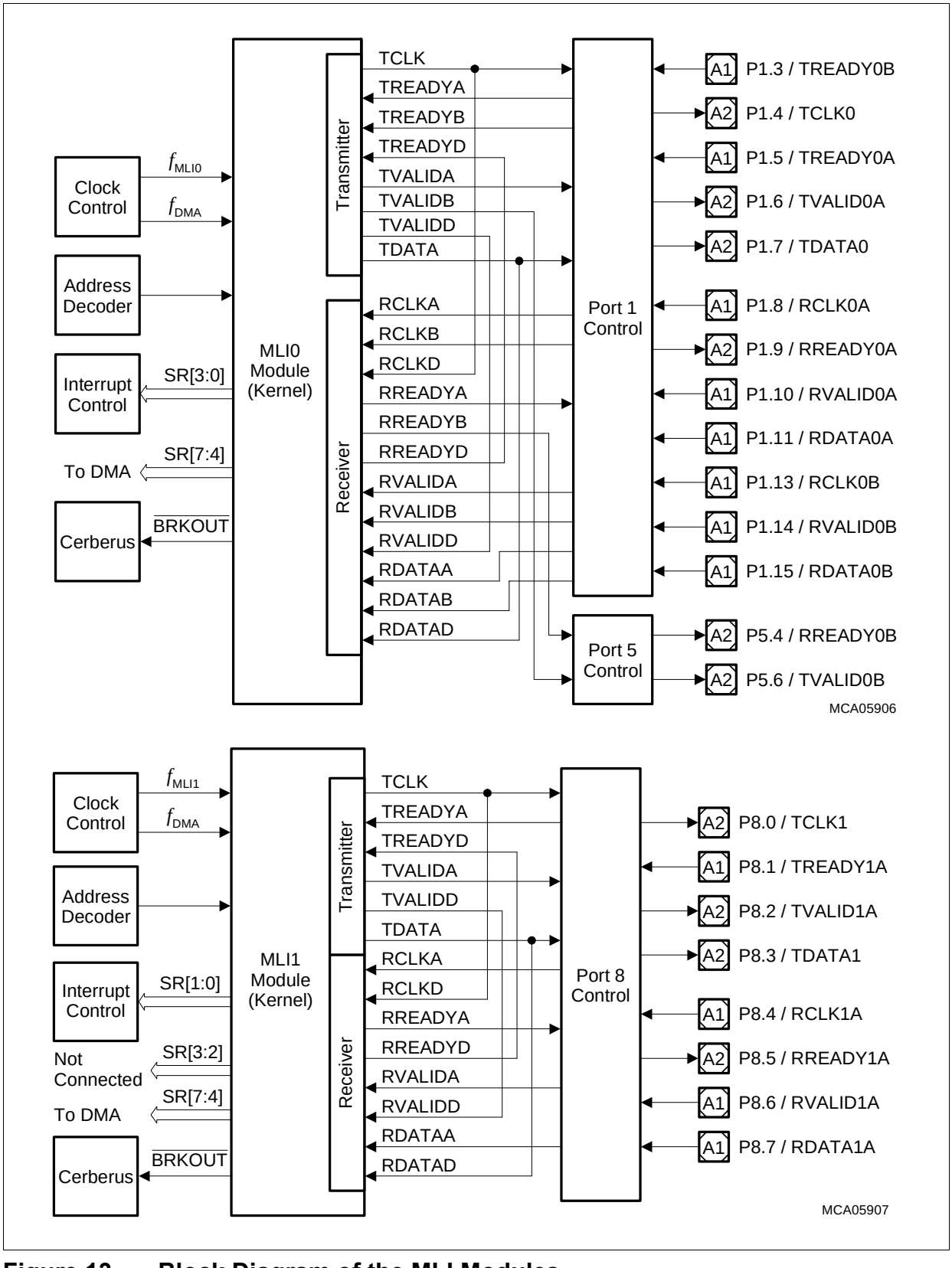


Figure 13 Block Diagram of the MLI Modules

3.14 General Purpose Timer Array

The GPTA provides a set of timer, compare and capture functionalities that can be flexibly combined to form signal measurement and signal generation units. They are optimized for tasks typical of engine, gearbox, and electrical motor control applications, but can also be used to generate simple and complex signal waveforms needed in other industrial applications.

The TC1796 contains two General Purpose Timer Arrays (GPTA0 and GPTA1) with identical functionality, plus an additional Local Timer Cell Array (LTCA2). **Figure 14** shows a global view of the GPTA modules.

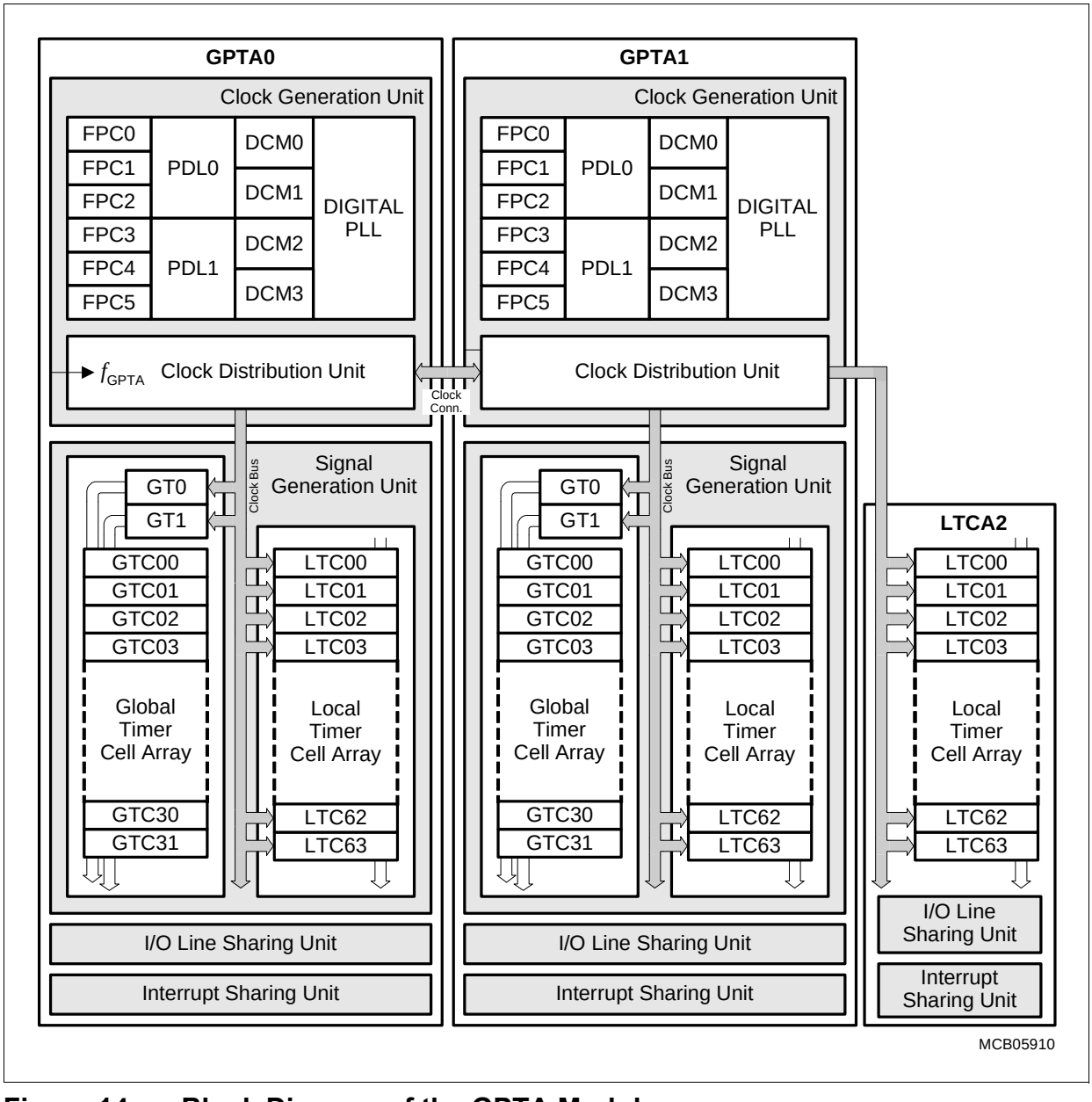


Figure 14 Block Diagram of the GPTA Modules

3.14.1 Functionality of GPTA0/GPTA1

Each of the General Purpose Timer Arrays (GPTA0 and GPTA1) provides a set of hardware modules required for high speed digital signal processing:

- Filter and Prescaler Cells (FPC) support input noise filtering and prescaler operation.
- Phase Discrimination Logic units (PDL) decode the direction information output by a rotation tracking system.
- Duty Cycle Measurement Cells (DCM) provide pulse-width measurement capabilities.
- A Digital Phase Locked Loop unit (PLL) generates a programmable number of GPTA module clock ticks during an input signal's period.
- Global Timer units (GT) driven by various clock sources are implemented to operate as a time base for the associated Global Timer Cells.
- Global Timer Cells (GTC) can be programmed to capture the contents of a Global Timer on an external or internal event. A GTC may be also used to control an external port pin depending on the result of an internal compare operation. GTCs can be logically concatenated to provide a common external port pin with a complex signal waveform.
- Local Timer Cells (LTC) operating in Timer, Capture, or Compare Mode may be also logically tied together to drive a common external port pin with a complex signal waveform. LTCs — enabled in Timer Mode or Capture Mode — can be clocked or triggered by various external or internal events.

Input lines can be shared by an LTC and a GTC to trigger their programmed operation simultaneously.

The following sections summarize the specific features of the GPTA units. The clock signal f_{GPTA} is the input clock of the GPTA modules (max. 75 MHz in TC1796).

Clock Generation Unit

- Filter and Prescaler Cell (FPC)
  - Six independent units
  - Three basic operating modes:
    Prescaler, Delayed Debounce Filter, Immediate Debounce Filter
  - Selectable input sources:
    Port lines, GPTA module clock, FPC output of preceding FPC cell
  - Selectable input clocks:
    GPTA module clock, prescaled GPTA module clock, DCM clock, compensated or uncompensated PLL clock.
  - f_{GPTA}/2 maximum input signal frequency in Filter Modes
- Phase Discriminator Logic (PDL)
  - Two independent units
  - Two operating modes (2 and 3 sensor signals)

  - f_{GPTA}/4 maximum input signal frequency in 2-sensor Mode, f_{GPTA}/6 maximum input signal frequency in 3-sensor Mode.
- Duty Cycle Measurement (DCM)
  - Four independent units
  - 0 - 100% margin and time-out handling
  - f_{GPTA} maximum resolution
  - f_{GPTA}/2 maximum input signal frequency
- Digital Phase Locked Loop (PLL)
  - One unit
  - Arbitrary multiplication factor between 1 and 65535
  - f_{GPTA} maximum resolution
  - f_{GPTA}/2 maximum input signal frequency
- Clock Distribution Unit (CDU)
  - One unit
  - Provides nine clock output signals:
    f_{GPTA}, divided f_{GPTA} clocks, FPC1/FPC4 outputs, DCM clock, LTC prescaler clock

Signal Generation Unit

- Global Timers (GT)
  - Two independent units
  - Two operating modes (Free Running Timer and Reload Timer)
  - 24-bit data width
  - f_{GPTA} maximum resolution
  - f_{GPTA}/2 maximum input signal frequency
- Global Timer Cell (GTC)
  - 32 units related to the Global Timers
  - Two operating modes (Capture, Compare and Capture after Compare)
  - 24-bit data width
  - f_{GPTA} maximum resolution
  - f_{GPTA}/2 maximum input signal frequency
- Local Timer Cell (LTC)
  - 64 independent units
  - Three basic operating modes (Timer, Capture and Compare) for 63 units
  - Special compare modes for one unit
  - 16-bit data width
  - f_{GPTA} maximum resolution
  - f_{GPTA}/2 maximum input signal frequency

Interrupt Sharing Unit

- 286 interrupt sources, generating up to 92 service requests

I/O Sharing Unit

- Interconnecting inputs and outputs from internal clocks, FPC, GTC, LTC, ports, and MSC interface.

3.14.2 Functionality of LTCA2

One Local Timer Cells Area provides a set of Local Timer Cells.

- 64 Local Timer Cells (LTCs)
  - Three basic operating modes (Timer, Capture and Compare) for 63 units.
  - Special compare modes for one unit
  - 16-bit data width
  - f_{GPTA} maximum resolution
  - f_{GPTA}/2 maximum input signal frequency

3.15 Analog-to-Digital Converter (ADC0, ADC1)

The two ADC modules of the TC1796 are analog to digital converters with 8-bit, 10-bit, or 12-bit resolution including sample & hold functionality.

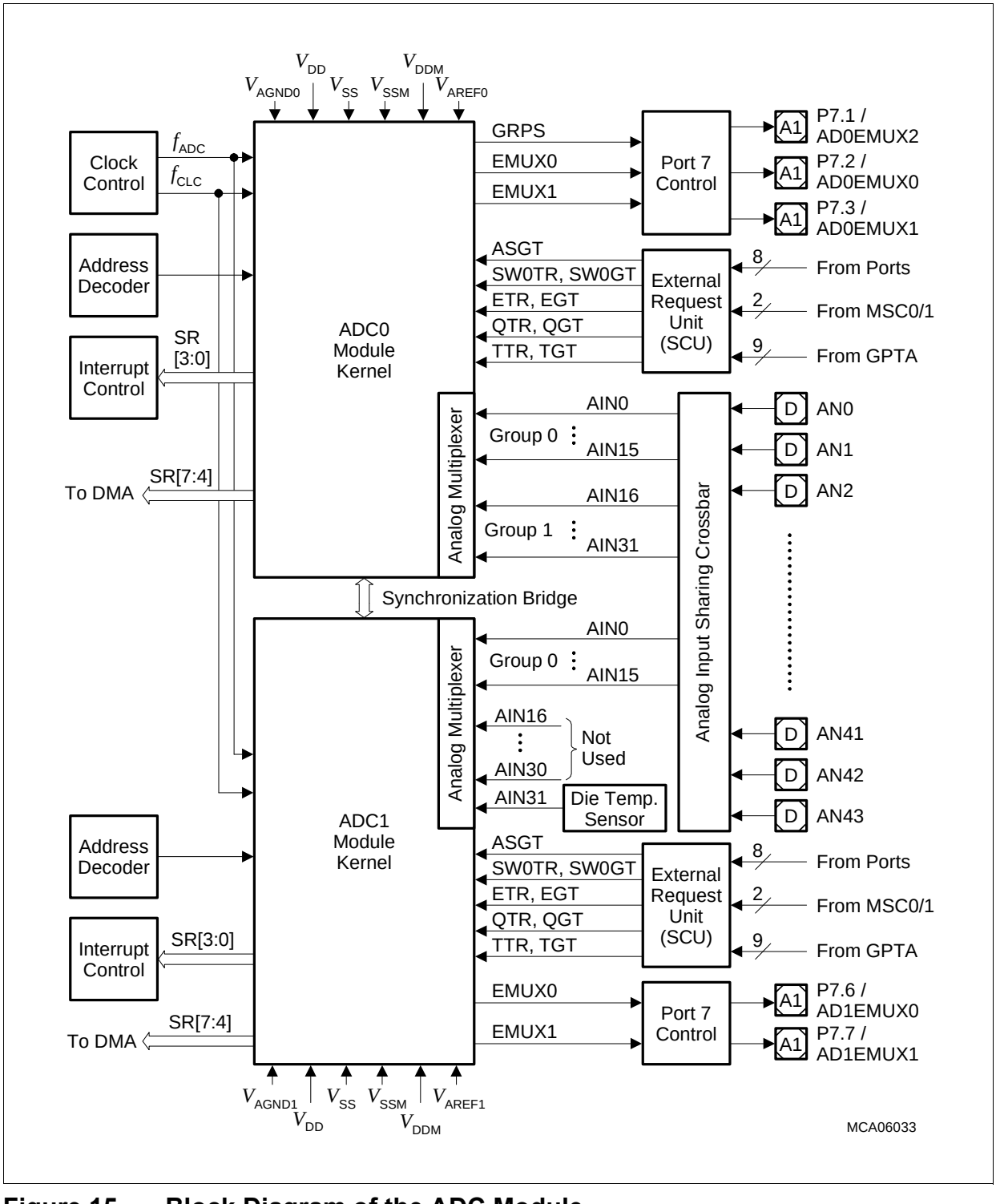


Figure 15 Block Diagram of the ADC Module

The A/D converters operate by the method of the successive approximation. A multiplexer selects between up to 32 analog inputs that can be connected with the 16 conversion channels in each ADC module. An automatic self-calibration adjusts the ADC modules to changing temperatures or process variations.

External Clock control, address decoding, and service request (interrupt) control is managed outside the ADC module kernel. A synchronization bridge is used for synchronization of two ADC modules. External trigger conditions are controlled by an External Request Unit. This unit generates the control signals for auto-scan control (ASGT), software trigger control (SW0TR, SW0GT), the event trigger control (ETR, EGT), queue control (QTR, QGT), and timer trigger control (TTR, TGT).

Features

- 8-bit, 10-bit, 12-bit A/D conversion
- Minimum conversion times (without sample time, @ 75 MHz module clock):
  - 1.05 µs @ 8-bit resolution
  - 1.25 µs @ 10-bit resolution
  - 1.45 µs @ 12-bit resolution
- Extended channel status information on request source
- Successive approximation conversion method
- Total Unadjusted Error (TUE) of ±2 LSB @ 10-bit resolution
- Integrated sample & hold functionality
- Direct control of up to 16(32) analog input channels per ADC
- Dedicated control and status registers for each analog channel
- Powerful conversion request sources
- Selectable reference voltages for each channel
- Programmable sample and conversion timing schemes
- Limit checking
- Flexible ADC module service request control unit
- Synchronization of the two on-chip A/D converters
- Automatic control of external analog multiplexers
- Equidistant samples initiated by timer
- External trigger and gating inputs for conversion requests
- Power reduction and clock control feature
- On-chip die temperature sensor output voltage measurement via ADC1

3.16 Fast Analog-to-Digital Converter Unit (FADC)

The FADC module of the TC1796 basically is a 4-channel A/D converter with 10-bit resolution that operates by the method of the successive approximation.

The main FADC functional blocks shown in **Figure 16** are:

- The Input Stage contains the differential inputs and the programmable amplifier.
- The A/D Converter is responsible for the analog-to-digital conversion.
- The Data Reduction Unit contains programmable anti aliasing and data reduction filters.
- The Channel Trigger Control block defines the trigger and gating conditions for the four FADC channels. The gating source inputs GS[7:0] and trigger source inputs TS[7:0] are connected with GPTA0 module outputs, with GPIO port lines, and external request unit outputs.
- The Channel Timers can independently trigger the conversion of each FADC channel.
- The A/D control block is responsible for the overall FADC functionality.

The FADC module is supplied by the following power supply and reference voltage lines:

- V_{DDMF}/V_{DDMF}: FADC Analog Part Power Supply (3.3V)
- V_{DDAF}/V_{DDAF}: FADC Analog Part Logic Power Supply (1.5V)
- V_{FAREF}/V_{FAGND}: FADC Reference Voltage/FADC Reference Ground

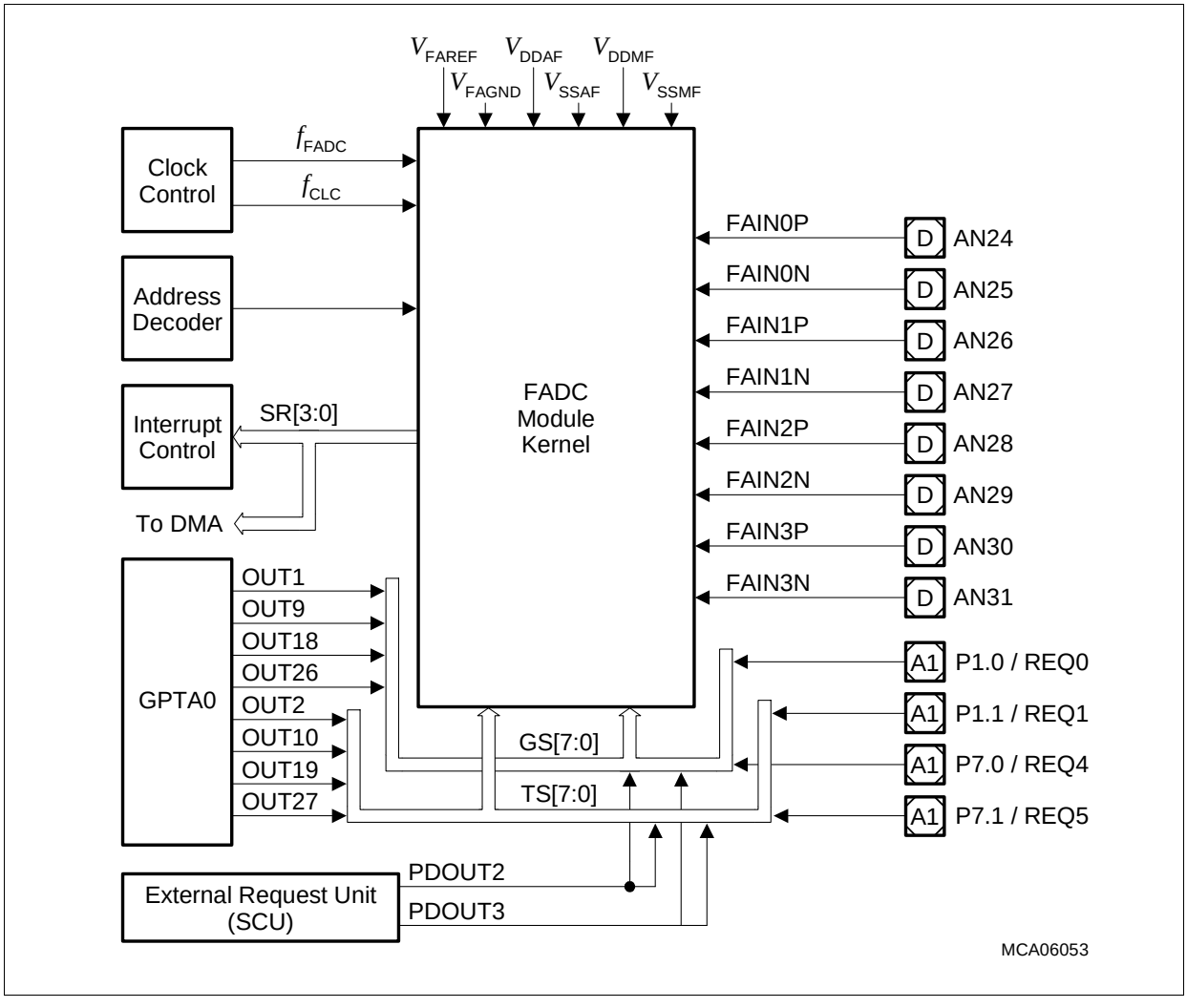


Figure 16 Block Diagram of the FADC Module

Features

- Extreme fast conversion: 21 cycles of f_{FADC} (= 280ns @ f_{FADC} = 75 MHz)
- 10-bit A/D conversion
  - Higher resolution by averaging of consecutive conversions is supported
- Successive approximation conversion method
- Four differential input channels
- Offset and gain calibration support for each channel
- Differential input amplifier with programmable gain of 1, 2, 4 and 8 for each channel
- Free-running (Channel Timers) or triggered conversion modes
- Trigger and gating control for external signals
- Built-in Channel Timers for internal triggering
- Channel timer request periods independently selectable for each channel
- Selectable, programmable anti aliasing and data reduction filter block

3.17 System Timer

The TC1796's STM is designed for global system timing applications requiring both high precision and long range.

Features

- Free-running 56-bit counter
- All 56 bits can be read synchronously
- Different 32-bit portions of the 56-bit counter can be read synchronously
- Flexible interrupt generation based on compare match with partial STM content
- Driven by max. 75 MHz (= f_{SYS}, default after reset = $f_{SYS}/2$)
- Counting starts automatically after a reset operation
- STM is reset by:
  - Watchdog reset
  - Software reset (RST_REQ.RRSTM must be set)
  - Power-on reset
- STM is not reset at a hardware reset
- STM can be halted in debug/suspend mode

The STM is an upward counter, running either at the system clock frequency f_{SYS} or at a fraction of it. In case of a power-on reset, a watchdog reset, or a software reset, the STM is reset. After one of these reset conditions, the STM is enabled and immediately starts counting up. It is not possible to affect the contents of the timer during normal operation of the TC1796. The timer registers can only be read but not written to. The STM can be optionally disabled or suspended for power-saving and debugging purposes via its clock control register. In suspend mode of the TC1796, the STM clock is stopped but all registers are still readable.

The System Timer can be read in sections from seven registers, STM_TIM0 through STM_TIM6, which select increasingly higher-order 32-bit ranges of the System Timer. These can be viewed as individual 32-bit timers, each with a different resolution and timing range. For getting a synchronous and consistent reading of the complete STM contents, a capture register (STM_CAP), is implemented. It latches the contents of the high part of the STM each time when one of the registers STM_TIM0 to STM_TIM5 is read. Thus, it holds the upper value of the timer at exactly the same time when the lower part is read. The second read operation would then read the contents of the STM_CAP to get the complete timer value.

The content of the 56-bit System Timer can be compared against the content of two compare values stored in the compare registers. Interrupts can be generated on a compare match of the STM with the STM_CMP0 or STM_CMP1 registers.

The maximum clock period is $2^{56} \times f_{STM}$. At f_{STM} = 75 MHz, for example, the STM counts 30.47 years before overflowing. Thus, it is capable of continuously timing the entire expected product life-time of a system without overflowing.

Figure 17 shows an overview on the System Timer with the options for reading parts of STM contents.

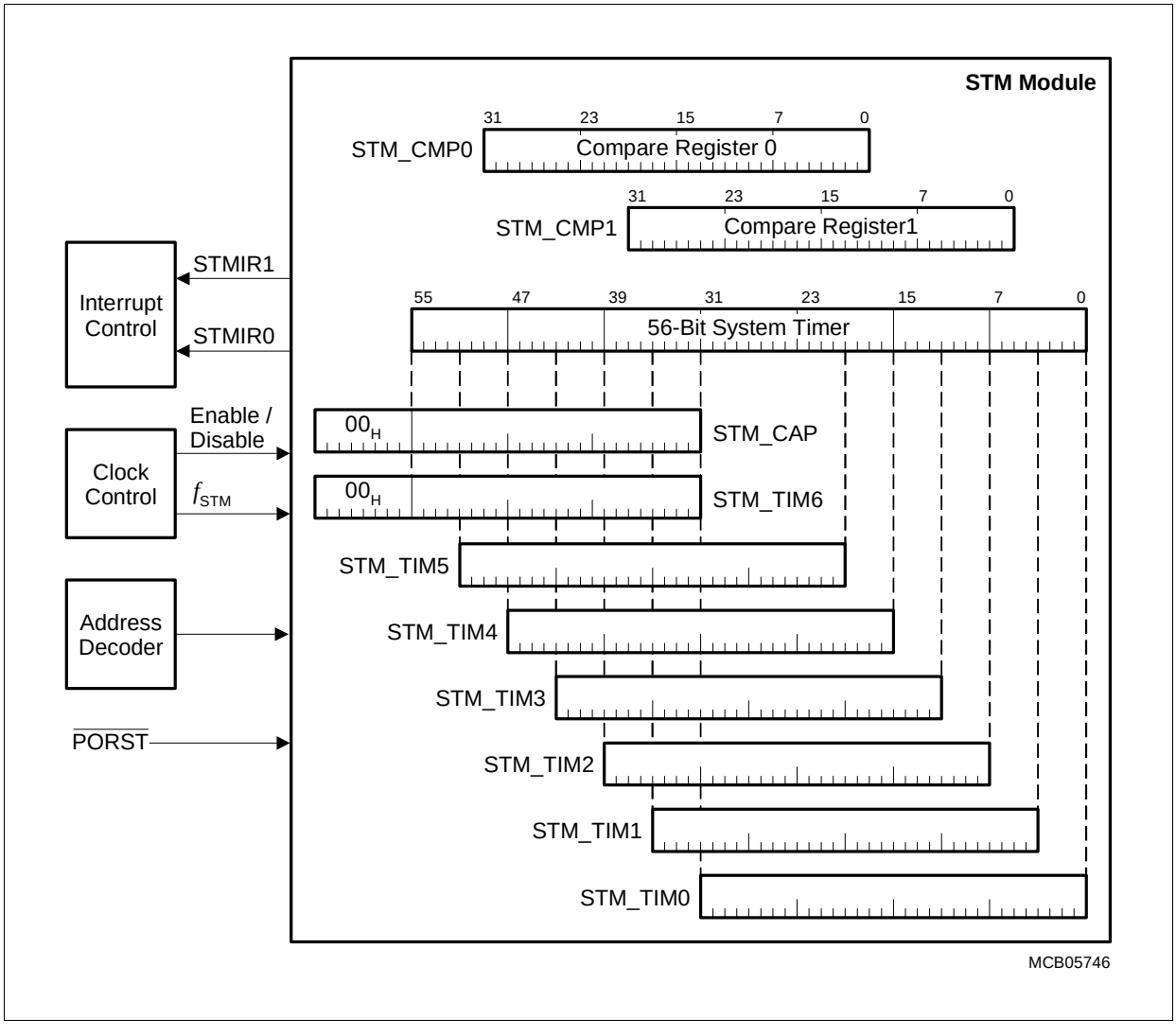


Figure 17 General Block Diagram of the STM Module Registers

3.18 Watchdog Timer

The Watchdog Timer (WDT) provides a highly reliable and secure way to detect and recover from software or hardware failure. The WDT helps to abort an accidental malfunction of the TC1796 in a user-specified time period. When enabled, the WDT will cause the TC1796 system to be reset if the WDT is not serviced within a user-programmable time period. The CPU must service the WDT within this time interval to prevent the WDT from causing a TC1796 system reset. Hence, routine service of the WDT confirms that the system is functioning properly.

In addition to this standard “Watchdog” function, the WDT incorporates the EndInit feature and monitors its modifications. A system-wide line is connected to the End-of-Initialization (Endinit) feature and monitors its modifications. A system-wide line is connected to the WDT_CON0.ENDINIT bit, serving as an additional write-protection for critical registers (besides Supervisor Mode protection)

A further enhancement in the TC1796’s WDT is its reset pre-warning operation. Instead of immediately resetting the device on the detection of an error (the way that standard Watchdogs do), the WDT first issues an Non-Maskable Interrupt (NMI) to the CPU before finally resetting the device at a specified time period later. This gives the CPU a chance to save system state to memory for later examination of the cause of the malfunction, an important aid in debugging.

Features

- 16-bit Watchdog counter
- Selectable input frequency: f_{SYS}/256 or f_{SYS}/16384
- 16-bit user-definable reload value for normal Watchdog operation, fixed reload value for Time-Out and Pre-warning Modes
- Incorporation of the ENDINIT bit and monitoring of its modifications
- Sophisticated password access mechanism with fixed and user-definable password fields
- Proper access always requires two write accesses. The time between the two accesses is monitored by the WDT and limited.
- Access Error Detection: Invalid password (during first access) or invalid guard bits (during second access) trigger the Watchdog reset generation.
- Overflow Error Detection: An overflow of the counter triggers the Watchdog reset generation.
- Watchdog function can be disabled; access protection and ENDINIT monitor function remain enabled.
- Double Reset Detection: If a Watchdog induced reset occurs twice, a severe system malfunction is assumed and the TC1796 is held in reset until a power-on reset. This prevents the device from being periodically reset if, for instance, connection to the external memory has been lost such that even system initialization could not be performed

- Important debugging support is provided through the reset pre-warning operation by first issuing an NMI to the CPU before finally resetting the device after a certain period of time.

3.19 System Control Unit

The System Control Unit (SCU) of the TC1796 handles several system control tasks. These system control tasks of the SCU are:

- Clock system selection and control
- Reset and boot operation control
- Power management control
- Configuration input sampling
- External Request Unit
- System clock output control
- Chip select generation for EBU
- EBU pull devices control
- On-chip SRAM Parity Control
- Pad driver temperature compensation control
- Emergency stop input control for GPTA outputs
- Die Temperature Sensor
- GPTA1 input IN0 control
- Pad Test Mode control for dedicated pins
- ODCS level 2 trace control
- NMI control
- Miscellaneous SCU control

3.20 Boot Options

The TC1796 booting schemes provide a number of different boot options for the start of code execution. **Table 7** shows the boot options available in the TC1796.

Table 7 TC1796 Boot Selections

BRKIN	HWCFG [3:0]	Type of Boot	Boot ROM Exit Jump Address
Normal Boot Options			
1	0000_B	Enter bootstrap loader mode 1: Serial ASC0 boot via ASC0 pins	$D400\ 0000_H$
	0001_B	Enter bootstrap loader mode 2: Serial CAN boot via CAN pins	
	0010_B	Start from internal PFLASH	$A000\ 0000_H$
	0011_B	Alternate boot mode (ABM): start from internal PFLASH after CRC check is correctly executed; enter a serial bootstrap loader mode[1] if CRC check fails.	As defined in ABM header or D400 0000H
	0100_B	Start from external memory with EBU as master, using $\overline{CS0}$; automatic EBU configuration[2];	$A100\ 0000_H$
	0101_B	Alternate boot mode (ABM): start from external memory with CRC check and EBU as master, using $\overline{CS0}$; enter a serial bootstrap loader mode[2] if CRC checks fails; automatic EBU configuration[2];	As defined in ABM header or D400 0000H
	0110_B	Start from external memory with EBU as participant, using $\overline{CS0}$; automatic EBU configuration[2];	$A100\ 0000_H$
	0111_B	Alternate boot mode (ABM): start from external memory with CRC check and EBU as participant, using $\overline{CS0}$; enter a serial bootstrap loader mode[2] if CRC checks fails; automatic EBU configuration[2];	As defined in ABM header or D400 0000H
	1000_B	Start from emulation memory if emulation device TC1796ED is available; in case of TC1796: Execute stop loop;	If TC1796ED: AFF0 0000H
	1111_B	Enter bootstrap loader mode 3: Serial ASC0 boot via CAN pins	$D400\ 0000_H$
	Others	Reserved; execute stop loop;	–

Table 7 TC1796 Boot Selections (cont'd)

BRKIN	HWCFG [3:0]	Type of Boot	Boot ROM Exit Jump Address
Debug Boot Options			
0	0000_B	Tri-state chip	–
	1000_B	Go to external emulator space with EBU as master, using CSEMU/CSCOMB	DE00 0000_H
	Others	Reserved; execute stop loop;	–

1) The type of the alternate bootstrap loader mode is selected by the value of the SCU_SCLIR.SWOPT[2:0] bit field, which contains the levels of the P0.[2:0] latched in with the rising edge of the HDRST. For more details on ABM, see the User's Manual.

2) The EBU fetches the boot configuration from address offset 4 using CS0.

3.21 Power Management System

The TC1796 power management system allows software to configure the various processing units so that they automatically adjust to draw the minimum necessary power for the application. There are three power management modes:

- Run Mode
- Idle Mode
- Sleep Mode

The operation of each system component in each of these states can be configured by software. The power-management modes provide flexible reduction of power consumption through a combination of techniques, including stopping the CPU clock, stopping the clocks of other system components individually, and individually clock-speed reduction of some peripheral components.

Besides these explicit software-controlled power-saving modes, in the TC1796 special attention has been paid for automatic power-saving in those operating units which are currently not required or idle. In that case they are shut off automatically until their operation is required again.

Table 8 describes the features of the power management modes.

Table 8 Power Management Mode Summary

Mode	Description
Run	The system is fully operational. All clocks and peripherals are enabled, as determined by software.
Idle	The CPU clock is disabled, waiting for a condition to return it to Run Mode. Idle Mode can be entered by software when the processor has no active tasks to perform. All peripherals remain powered and clocked. Processor memory is accessible to peripherals. A reset, Watchdog Timer event, a falling edge on the NMI pin, or any enabled interrupt event will return the system to Run Mode.
Sleep	The system clock signal is distributed only to those peripherals programmed to operate in Sleep Mode. The other peripheral module will be shut down by the suspend signal. Interrupts from operating peripherals, the Watchdog Timer, a falling edge on the NMI pin, or a reset event will return the system to Run Mode. Entering this state requires an orderly shut-down controlled by the Power Management State Machine.

In typical operation, Idle Mode and Sleep Mode may be entered and exited frequently during the run time of an application. For example, system software will typically cause the CPU to enter Idle Mode each time it has to wait for an interrupt before continuing its tasks. In Sleep Mode and Idle Mode, wake-up is performed automatically when any enabled interrupt signal is detected, or if the Watchdog Timer signals the CPU with an NMI trap.

3.22 On-Chip Debug Support

Figure 18 shows a block diagram of the TC1796 OCDS system.

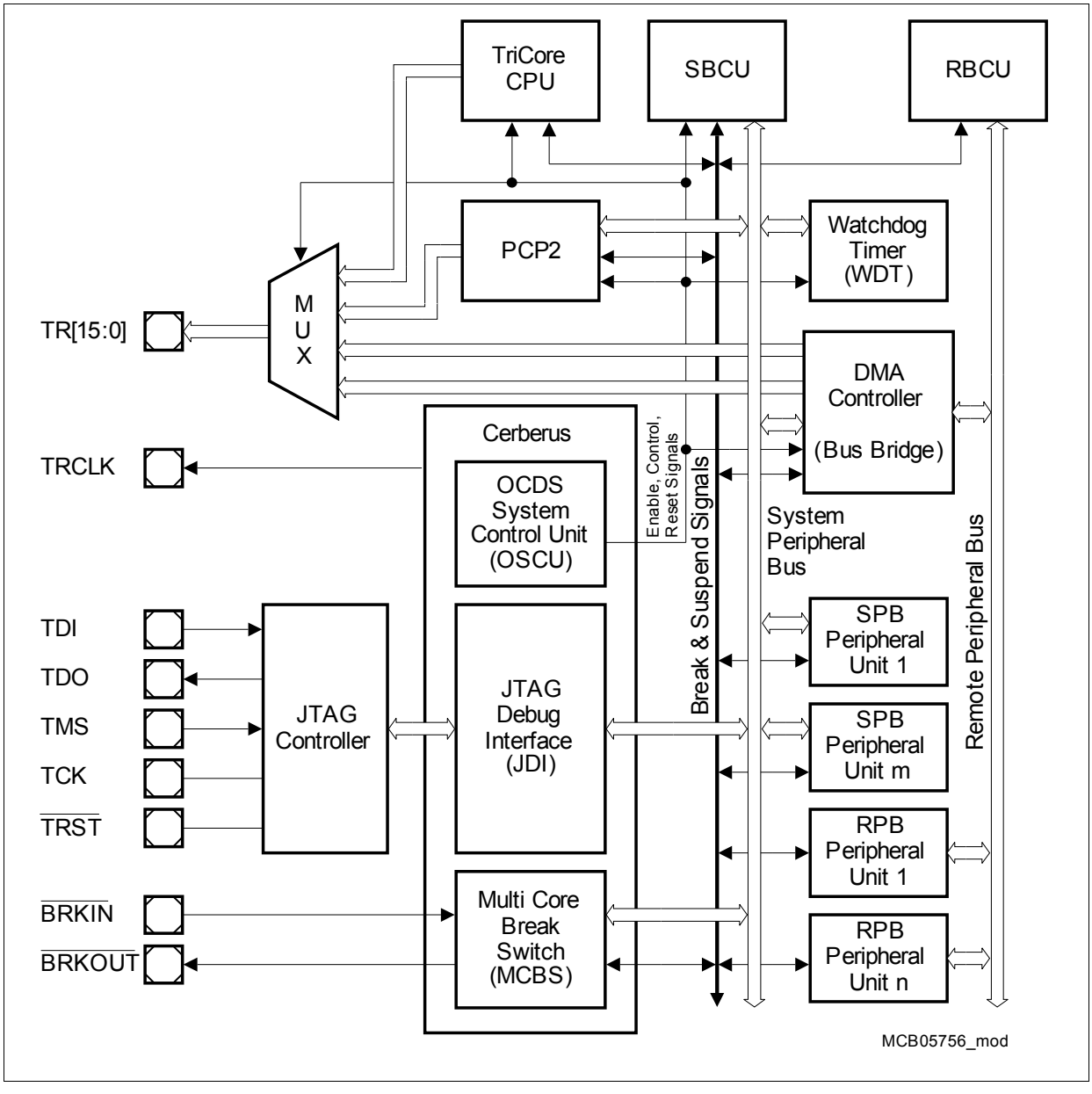


Figure 18 OCDS System Block Diagram

The TC1796 basically supports three levels of debug operation:

- OCDS Level 1 debug support
- OCDS Level 2 debug support
- OCDS Level 3 debug support

OCDS Level 1 Debug Support

The OCDS Level 1 debug support is mainly assigned for real-time software debugging purposes which have a demand for low-cost standard debugger hardware.

The OCDS Level 1 debug support is based on a JTAG interface which can be used by the external debug hardware to communicate with the system. The on-chip Cerberus module controls the interactions between the JTAG interface and the on-chip modules. The external debug hardware may become master of the internal buses and read or write the on-chip register/memory resources. The Cerberus also allows to define breakpoint and trigger conditions as well as to control user program execution (run/stop, break, single-step).

OCDS Level 2 Debug Support

The OCDS Level 2 debug support allows to implement program tracing capabilities for enhanced debuggers by extending the OCDS Level 1 debug functionality with an additional 16-bit wide trace port with trace clock. With the trace extension the following four trace capabilities are provided (only one of the four trace capabilities can be selected at a time):

- Trace capability of the CPU program flow
- Trace capability of the PCP2 program flow
- Trace capability of the DMA Controller transaction requests
- Trace capability of the DMA Controller move engine status information

OCDS Level 3 Debug Support

The OCDS Level 3 debug support is based on a special emulation device, the TC1796ED, which provides additional features required for high-end emulation purposes. The TC1796ED is a device which includes the TC1796 product chip and additional emulation extension hardware in a package with the same footprint as the TC1796.

3.23 Clock Generation and PLL

The TC1796 clock system performs the following functions:

- Acquires and buffers incoming clock signals to create a master clock frequency
- Distributes in-phase synchronized clock signals throughout the TC1796's entire clock tree
- Divides a system master clock frequency into lower frequencies required by the different modules for operation.
- Dynamically reduces power consumption during operation of functional units
- Statically reduces power consumption through programmable power-saving modes
- Reduces electromagnetic interference (EMI) by switching off unused modules

The clock system must be operational before the TC1796 is able to run. Therefore, it also contains special logic to handle power-up and reset operations. Its services are fundamental to the operation of the entire system, so it contains special fail-safe logic.

Features

- PLL operation for multiplying clock source by different factors
- Direct drive capability for direct clocking
- Comfortable state machine for secure switching between basic PLL, direct or prescaler operation
- Sleep and Power-Down Mode support

The TC1796 Clock Generation Unit (CGU) as shown in **Figure 19** allows a very flexible clock generation. It basically consists of an main oscillator circuit and a Phase- Locked Loop (PLL). The PLL can converts a low-frequency external clock signal from the oscillator circuit to a high-speed internal clock for maximum performance.

The system clock f_{SYS} is generated from an oscillator clock f_{OSC} in either of four hardware/software selectable ways:

- **Direct Drive Mode (PLL Bypass):**
  In Direct Drive Mode, the PLL is bypassed and the CGU clock outputs are directly fed from the clock signal f_{OSC}, i.e. $f_{CPU} = f_{OSC}$ and $f_{SYS} = f_{OSC}/2$ or f_{OSC}. This allows operation of the TC1796 with a reasonably small fundamental mode crystal.
- **VCO Bypass Mode (Prescaler Mode):**
  In VCO Bypass Mode, f_{CPU} and f_{SYS} are derived from f_{OSC} by the two divider stages, P-Divider and K-Divider. The system clock f_{SYS} can be equal to f_{CPU} or $f_{CPU}/2$.
- **PLL Mode:**
  In PLL Mode, the PLL is running. The VCO clock f_{VCO} is derived from f_{OSC}, divided by the P factor, multiplied by the PLL (N-Divider). The clock signals f_{CPU} and f_{SYS} are derived from f_{VCO} by the K-Divider. The system clock f_{SYS} can be equal to f_{CPU} or $f_{CPU}/2$.
- **PLL Base Mode:**
  In PLL Base Mode, the PLL is running at its VCO base frequency and f_{CPU} and f_{SYS}

are derived from f_{VCO} only by the K-Divider. In this mode, the system clock f_{SYS} can be equal to f_{CPU} or $f_{CPU}/2$.

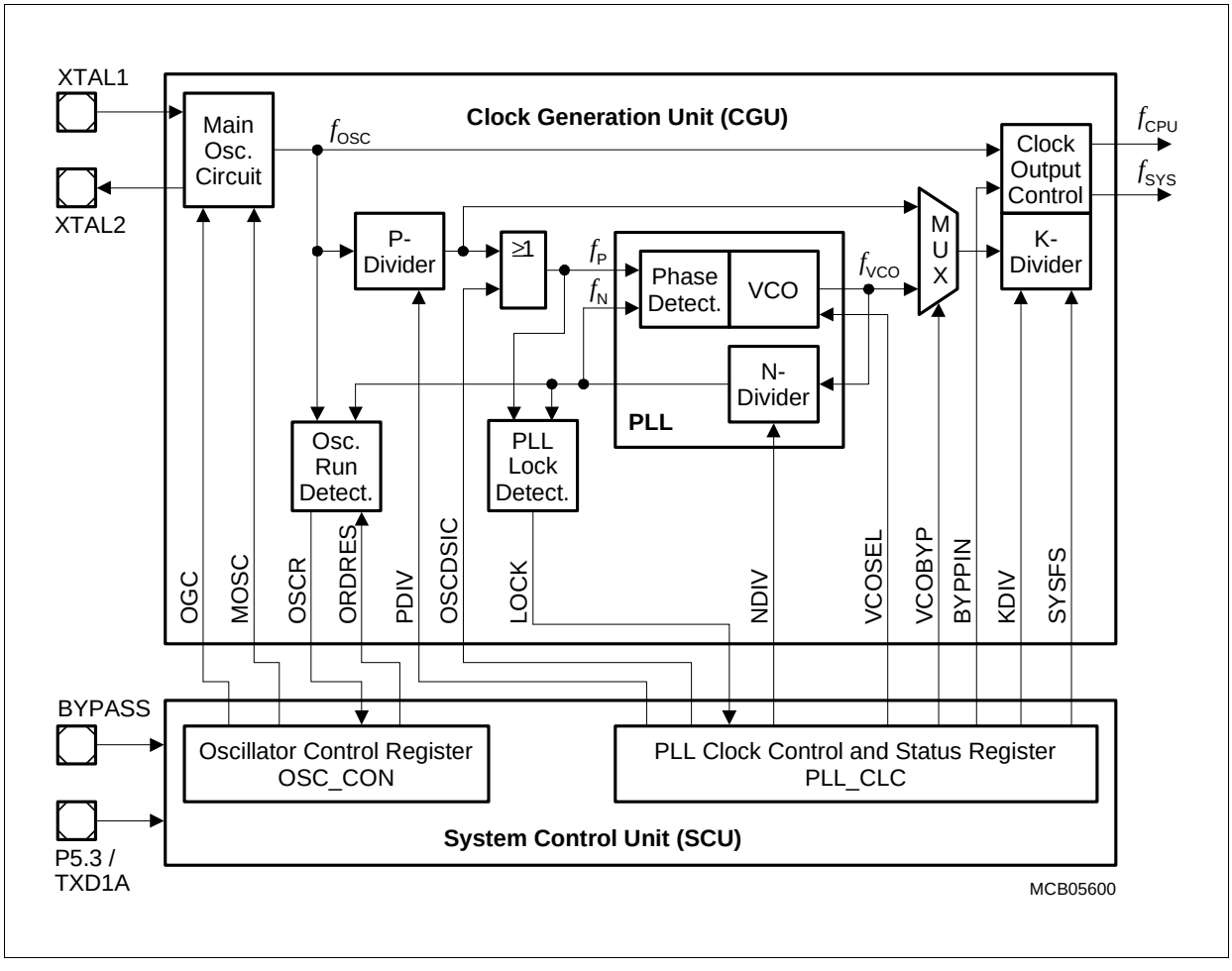


Figure 19 Clock Generation Unit

Recommended Oscillator Circuits

The oscillator circuit, a Pierce oscillator, is designed to work with both, an external crystal oscillator or an external stable clock source. It basically consists of an inverting amplifier and a feedback element with XTAL1 as input, and XTAL2 as output.

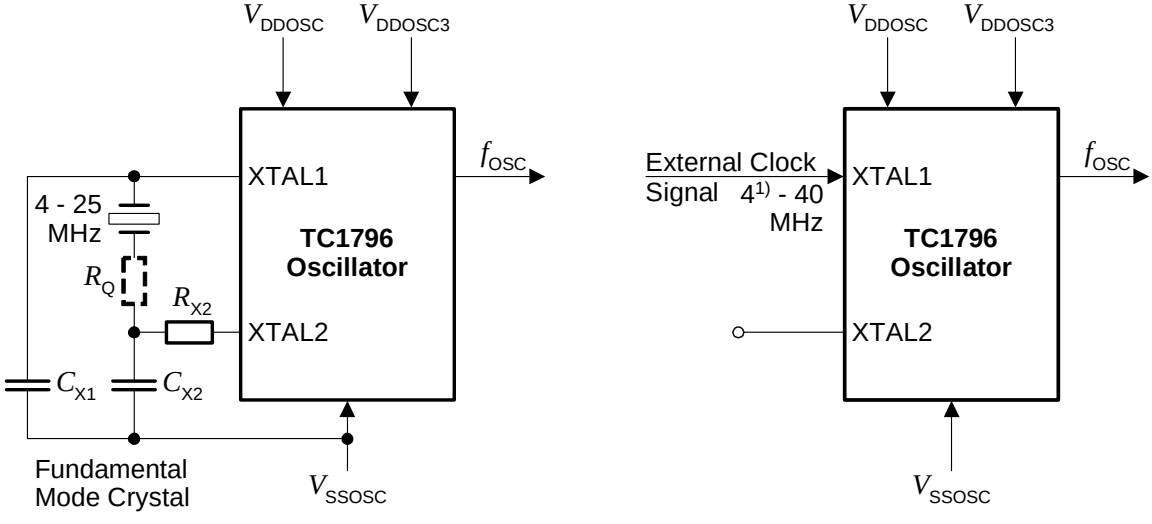
When using a crystal, a proper external oscillator circuitry must be connected to both pins, XTAL1 and XTAL2. The crystal frequency can be within the range of 4 MHz to 25 MHz. Additionally are necessary, two load capacitances C_{X1} and C_{X2}, and depending on the crystal type a series resistor R_{X2} to limit the current. A test resistor R_Q may be temporarily inserted to measure the oscillation allowance (negative resistance) of the oscillator circuitry. R_Q values are typically specified by the crystal vendor. The C_{X1} and C_{X2} values shown in **Figure 20** can be used as starting points for the negative resistance evaluation and for non-productive systems. The exact values and related operating range are dependent on the crystal frequency and have to be determined and

optimized together with the crystal vendor using the negative resistance method. Oscillation measurement with the final target system is strongly recommended to verify the input amplitude at XTAL1 and to determine the actual oscillation allowance (margin negative resistance) for the oscillator-crystal system.

When using an external clock signal, it must be connected to XTAL1. XTAL2 is left open (unconnected). The external clock frequency can be in the range of 0 - 40 MHz if the PLL is bypassed and 4 - 40 MHz if the PLL is used.

The oscillator can also be used in combination with a ceramic resonator. The final circuitry must be also verified by the resonator vendor.

Figure 20 shows the recommended external oscillator circuitries for both operating modes, external crystal mode and external input clock mode.



Crystal Frequency	C_{X1}, C_{X2} 1)	R_{X2} 1)
4 MHz	33 pF	0
8 MHz	18 pF	0
12 MHz	12 pF	0
16 - 25 MHz	10 pF	0

1) Note that these are evaluation start values!

MCS05601

Figure 20 Oscillator Circuitries

A block capacitor between V_{DDOSC} [1)]/V_{DDOSC3} and V_{SSOSC} is recommended, too.

Note: For crystal operation, it is strongly recommended to measure the negative resistance in the final target system (layout) to determine the optimum parameters

1) V_{DDOSC} and V_{SSOSC} are not bonded externally in the BC and BD steps of TC1796. An option for bonding them in future steps and products is kept open.

for the oscillator operation. Please refer to the minimum and maximum values of the negative resistance specified by the crystal supplier.

3.24 Power Supply

The TC1796 has several power supply lines for different voltage classes:

- 1.5 V: Core logic and memory, oscillator, and A/D converter supply
- 3.3 V: I/O ports, Flash memories, oscillator, and A/D converter supply with reference voltages
- 2.3 V to 3.3 V: External bus interface supply

Figure 21 shows the power supply concept of the TC1796 with the power supply pins and its connections to the functional units.

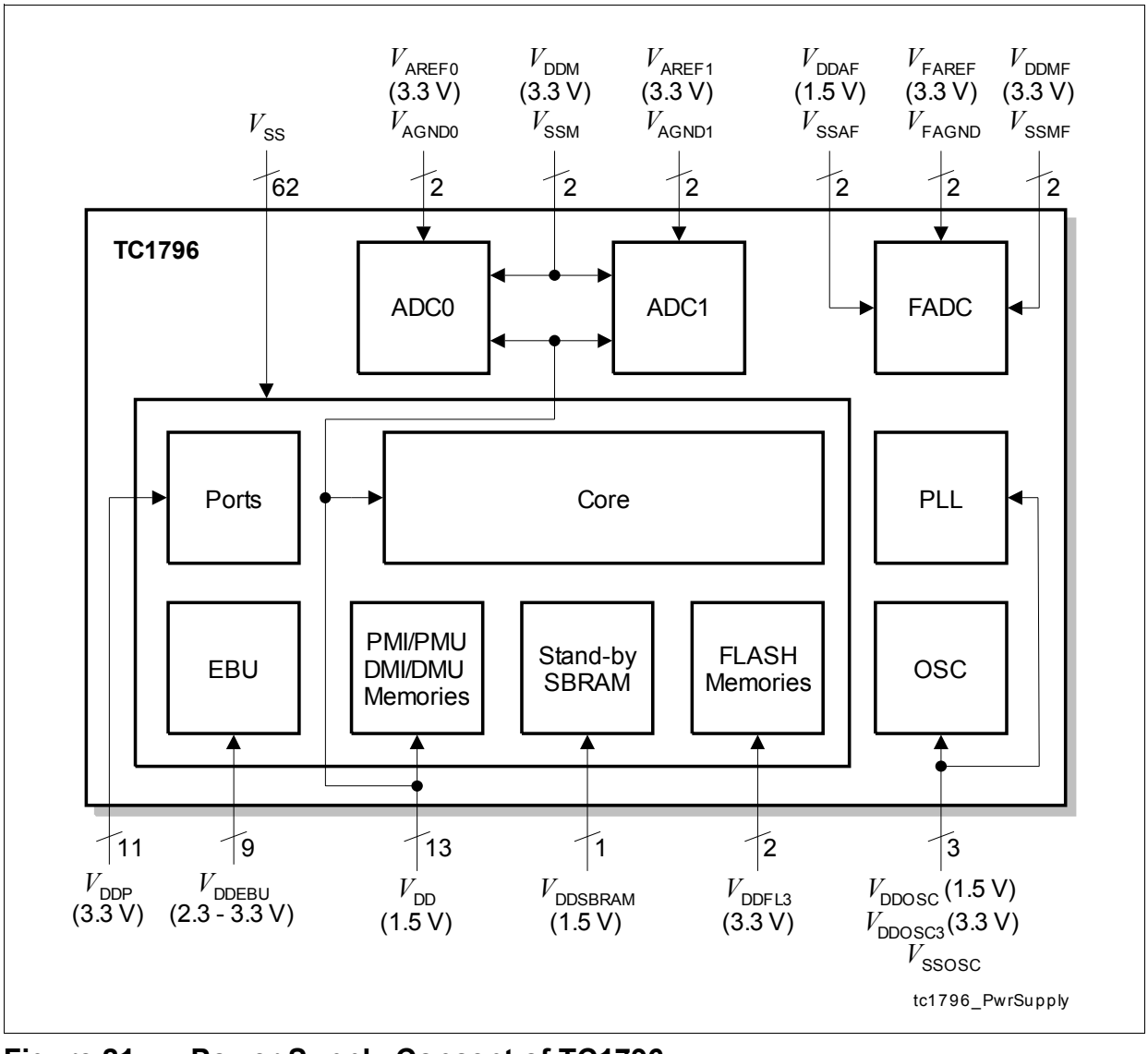


Figure 21 Power Supply Concept of TC1796

3.25 Identification Register Values

The Identification Registers uniquely identify a module or the whole device.

Table 9 TC1796 Identification Registers

Short Name	Address	Value	Stepping
SCU_ID	F000 0008$_H$	002C C002$_H$	–
MANID	F000 0070$_H$	0000 1820$_H$	–
CHIPID	F000 0074$_H$	0000 8A02$_H$	–
RTID	F000 0078$_H$	0000 0000$_H$	BA-Step
		0000 0001$_H$	BB-Step
		0000 0100$_H$	BC-Step
		0000 0101$_H$	BD-Step
		0000 0300$_H$	BE-Step
SBCU_ID	F000 0108$_H$	0000 6A0A$_H$	–
STM_ID	F000 0208$_H$	0000 C006$_H$	–
CBS_JPDID	F000 0408$_H$	0000 6307$_H$	–
MSC0_ID	F000 0808$_H$	0028 C002$_H$	–
MSC1_ID	F000 0908$_H$	0028 C002$_H$	–
ASC0_ID	F000 0A08$_H$	0000 4402$_H$	–
ASC1_ID	F000 0B08$_H$	0000 4402$_H$	–
GPTA0_ID	F000 1808$_H$	0029 C003$_H$	BA-, BB-Step
		0029 C004$_H$	BC-, BD-, BE-Step
GPTA1_ID	F000 2008$_H$	0029 C003$_H$	BA-, BB-Step
		0029 C004$_H$	BC-, BD-, BE-Step
LTCA2_ID	F000 2808$_H$	002A C003$_H$	BA-, BB-Step
		002A C004$_H$	BC-, BD-, BE-Step
DMA_ID	F000 3C08$_H$	001A C002$_H$	–
CAN_ID	F000 4008$_H$	002B C002$_H$	–
PCP_ID	F004 3F08$_H$	0020 C003$_H$	–
RBCU_ID	F010 0008$_H$	0000 6A0A$_H$	–
SSC0_ID	F010 0108$_H$	0000 4530$_H$	–
SSC1_ID	F010 0208$_H$	0000 4510$_H$	–
FADC_ID	F010 0308$_H$	0027 C002$_H$	–

Table 9 TC1796 Identification Registers (cont'd)

Short Name	Address	Value	Stepping
ADC0_ID	F010 0408$_H$	0030 C002$_H$	–
MLI0_ID	F010 C008$_H$	0025 C005$_H$	–
MLI1_ID	F010 C108$_H$	0025 C005$_H$	–
MCHK_ID	F010 C208$_H$	001B C001$_H$	–
CPS_ID	F7E0 FF08$_H$	0015 C006$_H$	–
CPU_ID	F7E1 FE18$_H$	000A C005$_H$	–
EBU_ID	F800 0008$_H$	0014 C005$_H$	–
PMU_ID	F800 0508$_H$	002E C002$_H$	–
FLASH_ID	F800 2008$_H$	0031 C002$_H$	–
DMU_ID	F801 0108$_H$	002D C002$_H$	–
DBCU_ID	F87F FA08$_H$	000F C005$_H$	–
DMI_ID	F87F FC08$_H$	0008 C004$_H$	–
PMI_ID	F87F FD08$_H$	000B C004$_H$	–
LFI_ID	F87F FF08$_H$	000C C005$_H$	–
PBCU_ID	F87F FE08$_H$	000F C005$_H$	–

4 Electrical Parameters

4.1 General Parameters

4.1.1 Parameter Interpretation

The parameters listed in this section partly represent the characteristics of the TC1796 and partly its requirements on the system. To aid interpreting the parameters easily when evaluating them for a design, they are marked with an two-letter abbreviation in column “Symbol”:

- **CC**
  Such parameters indicate **C**ontroller **C**haracteristics which are a distinctive feature of the TC1796 and must be regarded for a system design.
- **SR**
  Such parameters indicate **S**ystem **R**equirements which must provided by the microcontroller system in which the TC1796 designed in.

4.1.2 Pad Driver and Pad Classes Summary

This section gives an overview on the different pad driver classes and its basic characteristics. More details (mainly DC parameters) are defined in the **Section 4.2.1**.

Table 10 Pad Driver and Pad Classes Overview

Class	Power Supply	Type	Sub Class	Speed Grade	Load	Leakage [1]	Termination
A	3.3V	LVTTL I/O, LVTTL output	**A1** (e.g. GPIO)	6 MHz	100 pF	500 nA	No
			A2 (e.g. serial I/Os)	40 MHz	50 pF	6 µA	Series termination recommended
			A3 (e.g. Trace Outputs, serial I/Os)	75 MHz	50 pF	6 µA	Series termination recommended (for f > 25 MHz)
			A4 (e.g. Trace Clock)	150 MHz	25 pF	6 µA	Series termination recommended
B	2.375 - 3.6V[2]	LVTTL I/O	B1 (e.g. External Bus Interface)	40 MHz	50 pF	6 µA	No
			B2 (e.g. Bus Clock)	75 MHz	35 pF		Series termination recommended (for f > 25 MHz)
C	3.3V	LVDS	–	50 MHz		–	Parallel termination[3], 100 Ω ± 10%
D	–	Analog inputs, reference voltage inputs					

1) Values are for T_{Jmax} = 150 °C.

2) AC characteristics for EBU pins are valid for 2.5 V ± 5% and 3.3 V ± 5%.

3) In applications where the LVDS pins are not used (disabled), these pins must be either left unconnected, or properly terminated with the differential parallel termination of 100 Ω ± 10%.

4.1.3 Absolute Maximum Ratings

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
During absolute maximum rating overload conditions (V_{IN} > related V_{DD} or V_{IN} < V_{SS}) the voltage on the related V_{DD} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

Table 11 Absolute Maximum Rating Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Ambient temperature	T_A	SR	-40	–	125	°C	Under bias
Storage temperature	T_{ST}	SR	-65	–	150	°C	–
Junction temperature	T_J	SR	-40	–	150	°C	Under bias
Voltage at 1.5 V power supply pins with respect to V_{SS} [1]	V_{DD}	SR	–	–	2.25	V	–
Voltage at 3.3 V power supply pins with respect to V_{SS} [2]	V_{DDEBU} V_{DDP}	SR	–	–	3.75	V	–
Voltage on any Class A input pin and dedicated input pins with respect to V_{SS}	V_{IN}	SR	-0.5	–	V_{DDP} + 0.5 or max. 3.7	V	Whatever is lower
Voltage on any Class B input pin with respect to V_{SS}	V_{IN}	SR	-0.5	–	V_{DDEBU} + 0.5 or max. 3.7	V	Whatever is lower
Voltage on any Class D analog input pin with respect to V_{AGND}	V_{AIN} V_{AREFx}	SR	-0.5	–	V_{DDM} + 0.5 or max. 3.7	V	Whatever is lower
Voltage on any Class D analog input pin with respect to V_{SSAF}	V_{AINF} V_{FAREF}	SR	-0.5	–	V_{DDMF} + 0.5 or max. 3.7	V	Whatever is lower
CPU & LMB Bus Frequency	f_{CPU}	SR	–	–	150[3]	MHz	–
FPI Bus Frequency	f_{SYS}	SR	–	–	75[3]	MHz	–

1) Applicable for V_{DD}, $V_{DDSBRAM}$, V_{DDOSC}, V_{DDPLL}, and V_{DDAF}.

2) Applicable for V_{DDP}, V_{DDEBU}, V_{DDFL3}, V_{DDM}, and V_{DDMF}.

3) The PLL jitter characteristics add to this value according to the application settings. See the PLL jitter parameters.

4.1.4 Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation of the TC1796. All parameters specified in the following table refer to these operating conditions, unless otherwise noticed.

The following operating conditions must not be exceeded in order to ensure correct operation of the TC1796. All parameters specified in the following table refer to these operating conditions, unless otherwise noted.

Table 12 Operating Condition Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Digital supply voltage[1]	V_{DD} V_{DDOSC}[2]	SR SR	1.42	–	1.58[3]	V	–
	V_{DDP} V_{DDOSC3}	SR SR	3.13	–	3.47[4]	V	For Class A pins (3.3V ± 5%)
	V_{DDEBU}	SR	2.375	–	3.47[4]	V	For Class B (EBU) pins
	V_{DDFL3}	SR	3.13	–	3.47[4]	V	–
	$V_{DDSBRAM}$[5]	SR	1.42	–	1.58[3]	V	–
Voltage on $V_{DDSBRAM}$ power supply pin to ensure data retention	V_{DR}	SR	1.0	–	–	V	[6]
Digital ground voltage	V_{SS}	SR	0	–	–	V	–
Ambient temperature under bias	T_A	SR	–	-40	+125	°C	–
Analog supply voltages	–		–	–	–	–	See separate specification **Page 92**, **Page 99**
CPU clock	f_{CPU}	SR	–[7]	–	150[8]	MHz	–
Short circuit current	I_{SC}	SR	-5	–	+5	mA	[9]
Absolute sum of short circuit currents of a pin group (see **Table 13**)	$\Sigma\|I_{SC}\|$	SR	–	–	20	mA	See note[10]
Inactive device pin current	I_{ID}	SR	-1	–	1	mA	Voltage on all power supply pins V_{DDx} = 0

Table 12 Operating Condition Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Absolute sum of short circuit currents of the device	$\Sigma\|I_{SC}\|$	SR	–	–	100	mA	See note[10)]
External load capacitance	C_L	SR	–	–	–	pF	Depending on pin class. See DC characteristics

1) Digital supply voltages applied to the TC1796 must be static regulated voltages which allow a typical voltage swing of ±5%.

2) V_{DDOSC} and V_{SSOSC} are not bonded externally in the BC and BD steps of TC1796. An option for bonding them in future steps and products is kept open.

3) Voltage overshoot up to 1.7 V is permissible at Power-Up and $\overline{\text{PORST}}$ low, provided the pulse duration is less than 100 µs and the cumulated summary of the pulses does not exceed 1 h.

4) Voltage overshoot to 4 V is permissible at Power-Up and $\overline{\text{PORST}}$ low, provided the pulse duration is less than 100 µs and the cumulated summary of the pulses does not exceed 1 h

5) The V_{DDSB} must be properly connected and supplied with power. If not, the TC1796 will not operate. In case of a stand-by operation, the core voltage must not float, but must be pulled low, in order to avoid internal cross-currents.

6) This applies only during power down state. During normal SRAM operation regular V_{DD} has to be applied.

7) The TC1796 uses a static design, so the minimum operation frequency is 0 MHz. Due to test time restriction no lower frequency boundary is tested, however.

8) The PLL jitter characteristics add to this value according to the application settings. See the PLL jitter parameters.

9) Applicable for digital outputs.

10) See additional document “TC1796 Pin Reliability in Overload“ for overload current definitions.

Table 13 Pin Groups for Overload/Short-Circuit Current Sum Parameter

Group	Pins
1	P4.[7:0]
2	P4.[14:8]
3	P4.15, SLSO[1:0], SCLK0, MTSR0, MRST0, $\overline{\text{SLSI0}}$
4	$\overline{\text{WAIT}}$, $\overline{\text{HOLD}}$, $\overline{\text{BC}}$[3:0], $\overline{\text{HLDA}}$, MR/$\overline{\text{W}}$, $\overline{\text{BAA}}$, $\overline{\text{CSCOMB}}$
5	$\overline{\text{CS}}$[3:0], $\overline{\text{RD}}$, RD/$\overline{\text{WR}}$, $\overline{\text{BREQ}}$, $\overline{\text{ADV}}$, BFCLKO
6	BFCLKI, D[31:24]
7	D[23:16]
8	D[15:8]

Table 13 Pin Groups for Overload/Short-Circuit Current Sum Parameter

Group	Pins
9	D[7:0]
10	A[23:16]
11	A[15:8]
12	A[7:0]
13	TSTRES, TDI, TMS, TCK, $\overline{\text{TRST}}$, TDO, $\overline{\text{BRKOUT}}$, $\overline{\text{BRKIN}}$, $\overline{\text{TESTMODE}}$
14	P10.[3:0], BYPASS, $\overline{\text{NMI}}$, $\overline{\text{PORST}}$, $\overline{\text{HDRST}}$
15	P9.[8:0]
16	FCLP[1:0]A, FCLN[1:0], SOP[1:0]A, SON[1:0]
17	P5.[7:0]
18	P3.[7:0]
19	P3.[15:8]
20	P0.[7:0]
21	P0.[15:8]
22	P2.[15:7]
23	P2.[6:2], P6.9, P6.8, P6.6, P6.11
24	P6.[15:12], P6.10, P6.7, P6.[5:4]
25	P8.[7:0]
26	P1.[15:13], P1.[11:8], P1.5
27	P1.12, P1.[7:6], P1.[4:0]
28	TR[15:8]
29	TR[7:1], TRCLK
30	TR0, P7.[7:0]

4.2 DC Parameters

4.2.1 Input/Output Pins

Table 14 Input/Output DC-Characteristics (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
General Parameters						
Pull-up current[1)]	$\lvert I_{PUH}\rvert$ CC	10	–	100	µA	$V_{IN} < V_{IHAmin}$; class A1/A2/Input pads.
		20	–	200	µA	$V_{IN} < V_{IHAmin}$; class A3/A4 pads.
		5	–	85	µA	$V_{IN} < V_{IHBmin}$; class B1/B2 pads.
Pull-down current[1)]	$\lvert I_{PDL}\rvert$ CC	10	–	150	µA	$V_{IN} > V_{ILAmax}$; class A1/A2/Input pads. $V_{IN} > V_{ILBmax}$; class B1/B2 pads
		20	–	200	µA	$V_{IN} > V_{ILAmax}$; class A3/A4 pads.
Pin capacitance[1)] (Digital I/O)	C_{IO} CC	–	–	10	pF	f = 1 MHz T_A = 25 °C
Input only Pads (V_{DDP} = 3.13 to 3.47 V = 3.3 V ± 5%)						
Input low voltage Class A1/A2 pins	V_{ILA} SR	-0.3	–	0.34 × V_{DDP}	V	–
Input high voltage Class A1/A2 pins	V_{IHA} SR	0.64 × V_{DDP}	–	V_{DDP}+ 0.3 or max. 3.6	V	Whatever is lower
Ratio V_{IL}/V_{IH}	CC	0.53	–	–	–	–
Input hysteresis	HYSA CC	0.1 × V_{DDP}	–	–	V	5)2)
Input leakage current	I_{OZI} CC	–	–	±3000 ±6000	nA	V_{DDP}/2-1 < V_{IN} < V_{DDP}/2+1 Otherwise[3)]

Table 14 Input/Output DC-Characteristics (cont'd)(Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Class A Pads (V_{DDP} = 3.13 to 3.47 V = 3.3V ± 5%)						
Output low voltage[4]	V_{OLA} CC	–	–	0.4	V	I_{OL} = 2 mA for strong driver mode, I_{OL} = 1.8 mA for medium driver mode, A2 pads I_{OL} = 1.4 mA for medium driver mode, A1 pads I_{OL} = 370 µA for weak driver mode
Output high voltage[3]	V_{OHA} CC	2.4	–	–	V	I_{OH} = -2 mA for strong driver mode, I_{OH} = -1.8 mA for medium driver mode, A1/A2 pads I_{OH} = -370 µA for weak driver mode
		V_{DDP} - 0.4	–	–	V	I_{OH} = -1.4 mA for strong driver mode, I_{OH} = -1 mA for medium driver mode, A1/A2 pads I_{OH} = -280 µA for weak driver mode
Input low voltage Class A1/2 pins	V_{ILA} SR	-0.3	–	0.34 × V_{DDP}	V	–
Input high voltage Class A1/2 pins	V_{IHA} SR	0.64 × V_{DDP}	–	V_{DDP} + 0.3 or 3.6	V	Whatever is lower
Ratio V_{IL}/V_{IH}	CC	0.53	–	–	–	–
Input hysteresis	HYSA CC	0.1 × V_{DDP}	–	–	V	[5][2]
Input leakage current Class A2/3/4 pins	I_{OZA24}	–	–	±3000 ±6000	nA	V_{DDP}/2-1 < V_{IN} < V_{DDP}/2+1 Otherwise[3]
Input leakage current Class A1 pins	I_{OZA1} CC	–	–	±500	nA	0 V < V_{IN} < V_{DDP}

Table 14 Input/Output DC-Characteristics (cont'd)(Operating Conditions apply)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Class B Pads (V_{DDEBU} = 2.375 to 3.47 V)							
Output low voltage	V_{OLB}	CC	–	–	0.4	V	I_{OL} = 2 mA
Output high voltage	V_{OHB}	CC	V_{DDEBU} - 0.4	–	–	V	I_{OL} = 2 mA
Input low voltage	V_{ILB}	SR	–	-0.3	0.34 × V_{DDEBU}	V	–
Input high voltage	V_{IHB}	SR	0.64 × V_{DDEBU}	–	V_{DDEBU} +0.3 or 3.6	V	Whatever is lower
Ratio V_{IL}/V_{IH}		CC	0.53	–	–	–	–
Input hysteresis	HYSB	CC	0.1 × V_{DDEBU}	–	–	V	5)
Input leakage current Class B pins	I_{OZB}	CC	–	–	±3000 ±6000	nA	V_{DDEBU}/2-0.6 < V_{IN} < V_{DDEBU}/2+0.6[6] Otherwise[3]
Class C Pads (V_{DDP} = 3.13 to 3.47 V = 3.3V ± 5%)							
Output low voltage	V_{OL}	CC	815	–		mV	Parallel termination 100 Ω ± 1%
Output high voltage	V_{OH}	CC		–	1545	mV	Parallel termination 100 Ω ± 1%
Output differential voltage	V_{OD}	CC	150	–	600	mV	Parallel termination 100 Ω ± 1%
Output offset voltage	V_{OS}	CC	1075	–	1325	mV	Parallel termination 100 Ω ± 1%
Output impedance	R_0	CC	40	–	140	Ω	–
Class D Pads							
See ADC Characteristics			–	–	–	–	–

1) Not subject to production test, verified by design / characterization.

2) The pads that have spike-filter function in the input path: $\overline{\text{PORST}}$, $\overline{\text{HDRST}}$, NMI, do not have hysteresis.

3) Only one of these parameters is tested, the other is verified by design characterization

4) Max. resistance between pin and next power supply pin 25 Ω for strong driver mode (verified by design characterization).

5) Function verified by design, value verified by design characterization.
Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce.
It cannot be guaranteed that it suppresses switching due to external system noise.

6) V_{DDEBU} = 2.5 V $\pm$ 5%. For V_{DDEBU} = 3.3 $\pm$ 5% see class A2 pads.

4.2.2 Analog to Digital Converters (ADC0/ADC1)

Table 15 ADC Characteristics (Operating Conditions apply)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Analog supply voltage	V_{DDM}	SR	3.13	3.3	3.47[1)]	V	–
	V_{DD}	SR	1.42	1.5	1.58[2)]	V	Power supply for ADC digital part, internal supply
Analog ground voltage	V_{SSM}	SR	-0.1	–	0.1	V	–
Analog reference voltage[17)]	V_{AREFx}	SR	V_{AGNDx} +1V	V_{DDM}	V_{DDM}+ 0.05 [1)3)4)]	V	–
Analog reference ground[17)]	V_{AGNDx}	SR	V_{SSMx} - 0.05V	0	V_{AREF} - 1V	V	–
Analog input voltage range	V_{AIN}	SR	V_{AGNDx}	–	V_{AREFx}	V	–
Analog reference voltage range[5)17)]	V_{AREFx}- V_{AGNDx}	SR	V_{DDM}/2	–	V_{DDM} + 0.05	V	–
V_{DDM} supply current	I_{DDM}	SR	–	2.5	4	mA rms	For each module[6)]
Power-up calibration time	t_{PUC}	CC	–	–	3840	f_{ADC} CLK	–
Internal ADC clocks	f_{BC}	CC	2	–	40	MHz	$f_{BC} = f_{ANA} \times 4$
	f_{ANA}	CC	0.5	–	10	MHz	$f_{ANA} = f_{BC} / 4$
Total unadjusted error[5)]	TUE[7)]	CC	–	–	±1	LSB	8-bit conversion.
			–	–	±2	LSB	10-bit conversion
			–	–	±4	LSB	12-bit conversion [8)9)]
			–	–	±8	LSB	12-bit conversion [10)9)]
DNL error[11) 5)]	TUE_{DNL}	CC	–	±1.5	±3.0	LSB	12-bit conversion [12)9)]
INL error[11)5)]	TUE_{INL}	CC	–	±1.5	±3.0	LSB	12-bit conversion [12)9)]

Table 15 ADC Characteristics (cont'd) (Operating Conditions apply)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Gain error[11)5)]	TUE_{GAIN}	CC	–	±0.5	±3.5	LSB	12-bit conversion [12)9)]
Offset error[11)5)]	TUE_{OFF}	CC	–	±1.0	±4.0	LSB	12-bit conversion [12)9)]
Input leakage current at analog inputs AN0, AN1, AN4 to AN7, AN24 to AN31. see **Figure 24** [13) 14)]	I_{OZ1}	CC	-1000	–	300	nA	(0% V_{DDM}) < V_{IN} < (2% V_{DDM})
			-200	–	400	nA	(2% V_{DDM}) < V_{IN} < (95% V_{DDM})
			-200	–	1000	nA	(95% V_{DDM}) < V_{IN} < (98% V_{DDM})
			-200	–	3000	nA	(98% V_{DDM}) < V_{IN} < (100% V_{DDM})
Input leakage current at the other analog inputs, that is AN2, AN3, AN8 to AN23, AN32 to AN43 see **Figure 24** [14)]	I_{OZ1}	CC	-1000	–	200	nA	(0% V_{DDM}) < V_{IN} < (2% V_{DDM})
			-200	–	300	nA	(2% V_{DDM}) < V_{IN} < (95% V_{DDM})
			-200	–	1000	nA	(95% V_{DDM}) < V_{IN} < (98% V_{DDM})
			-200	–	3000	nA	(98% V_{DDM}) < V_{IN} < (100% V_{DDM})
Input leakage current at V_{AREF}	I_{OZ2}	CC	–	–	±1	µA	0 V < V_{AREF} < V_{DDM}, no conversion running
Input current at $V_{AREF0/1}$[17)]	I_{AREF}	CC	–	35	75	µA rms	0 V < V_{AREF} < V_{DDM}[15)]
Total capacitance of the voltage reference inputs[16)17)]	$C_{AREFTOT}$	CC	–	–	25	pF	[9)]
Switched capacitance at the positive reference voltage input[17)]	C_{AREFSW}	CC	–	15	20	pF	[9)18)]

Table 15 ADC Characteristics (cont'd) (Operating Conditions apply)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Resistance of the reference voltage input path[16)]	R_{AREF}	CC	–	1	1.5	kΩ	500 Ohm increased for AN[1:0] used as reference input[9)]
Total capacitance of the analog inputs[16)]	C_{AINTOT}	CC	–	–	25	pF	6)9)
Switched capacitance at the analog voltage inputs	C_{AINSW}	CC	–	–	7	pF	9)19)
ON resistance of the transmission gates in the analog voltage path	R_{AIN}	CC	–	1	1.5	kΩ	9)
ON resistance for the ADC test (pull-down for AIN7)	R_{AIN7T}	CC	200	300	1000	Ω	Test feature available only for AIN7[9)]
Current through resistance for the ADC test (pull-down for AIN7)	I_{AIN7T}	CC	–	15 rms	30 peak	mA	Test feature available only for AIN7[9)]

1) Voltage overshoot to 4 V are permissible, provided the pulse duration is less than 100 µs and the cumulated summary of the pulses does not exceed 1 h.

2) Voltage overshoot to 1.7 V are permissible, provided the pulse duration is less than 100 µs and the cumulated summary of the pulses does not exceed 1 h.

3) A running conversion may become inexact in case of violating the normal operating conditions (voltage overshoot).

4) If the reference voltage V_{AREF} increases or the V_{DDM} decreases, so that V_{AREF} = (V_{DDM} + 0.05V to V_{DDM} + 0.07V), then the accuracy of the ADC decreases by 4LSB12.

5) If a reduced reference voltage in a range of V_{DDM}/2 to V_{DDM} is used, then the ADC converter errors increase. If the reference voltage is reduced with the factor k (k<1), then TUE, DNL, INL Gain and Offset errors increase with the factor 1/k.
If a reduced reference voltage in a range of 1 V to V_{DDM}/2 is used, then there are additional decrease in the ADC speed and accuracy.

6) Current peaks of up to 6 mA with a duration of max. 2 ns may occur

7) TUE is tested at V_{AREF} = 3.3 V, V_{AGND} = 0 V and V_{DDM} = 3.3 V

8) ADC module capability.
9) Not subject to production test, verified by design / characterization.
10) Value under typical application conditions due to integration (switching noise, etc.).
11) The sum of DNL/INL/Gain/Offset errors does not exceed the related TUE total unadjusted error.
12) For 10-bit conversions the DNL/INL/Gain/Offset error values must be multiplied with factor 0.25.
For 8-bit conversions the DNL/INL/Gain/Offset error values must be multiplied with 0.0625.
13) The leakage current definition is a continuous function, as shown in **Figure 24**. The numerical values defined determine the characteristic points of the given continuous linear approximation - they do not define step function.
14) Only one of these parameters is tested, the other is verified by design characterization.
15) I_{AREF_MAX} is valid for the minimum specified conversion time. The current flowing during an ADC conversion with a duration of up to t_C = 25µs can be calculated with the formula $I_{AREF\_MAX} = Q_{CONV}/t_C$. Every conversion needs a total charge of Q_{CONV} = 150pC from V_{AREF}.
All ADC conversions with a duration longer than t_C = 25µs consume an I_{AREF_MAX} = 6µA.
16) For the definition of the parameters see also **Figure 23**.
17) Applies to AIN0 and AIN1, when used as auxiliary reference inputs.
18) This represents an equivalent switched capacitance. This capacitance is not switched to the reference voltage at once. Instead of this smaller capacitances are successively switched to the reference voltage.
19) The sampling capacity of the conversion C-Network is pre-charged to V_{AREF}/2 before the sampling moment. Because of the parasitic elements the voltage measured at AINx is lower then V_{AREF}/2, typically 0.85V.

Table 16 Sample and Conversion Time (Operating Conditions apply)

Parameter	Symbol		Values			Unit	Note
			Min.	Typ.	Max.		
Sample time	t_S	CC	$4 \times (CHCONn.STC + 2) \times t_{BC}$			µs	–
			$8 \times t_{BC}$	–	–	µs	–
Conversion time	t_C	CC	$t_S + 40 \times t_{BC} + 2 \times t_{DIV}$			µs	8-bit conversion
			$t_S + 48 \times t_{BC} + 2 \times t_{DIV}$			µs	10-bit conversion
			$t_S + 56 \times t_{BC} + 2 \times t_{DIV}$			µs	12-bit conversion

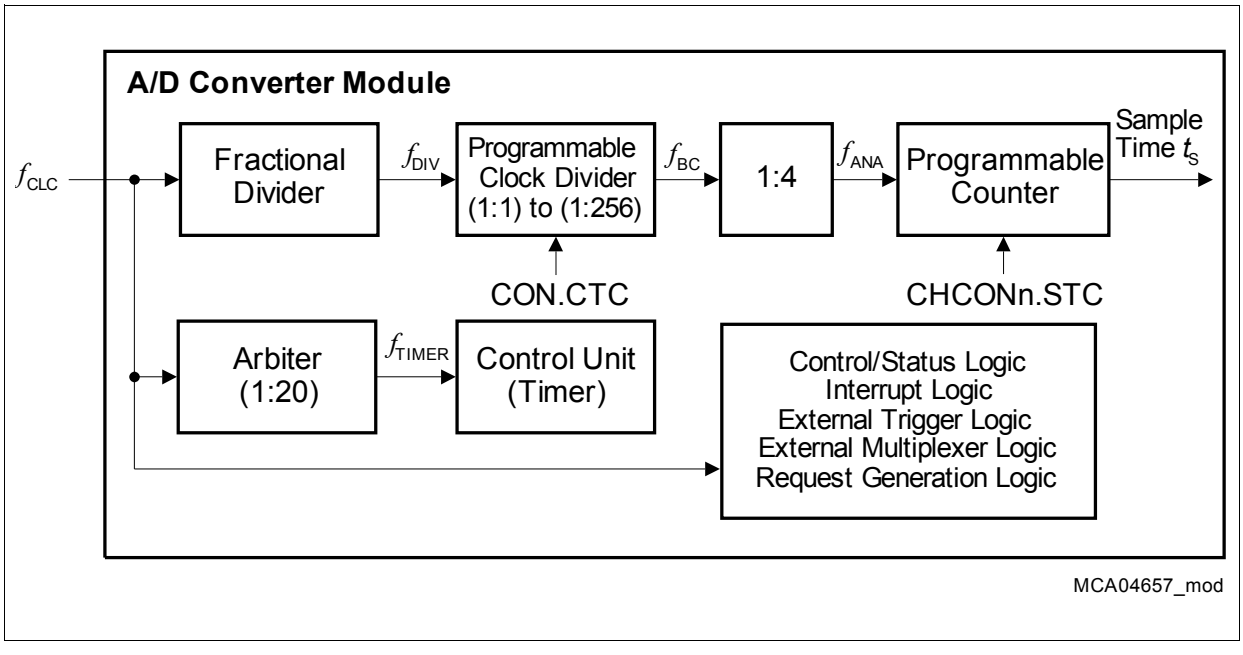


Figure 22 ADC0/ADC1 Clock Circuit

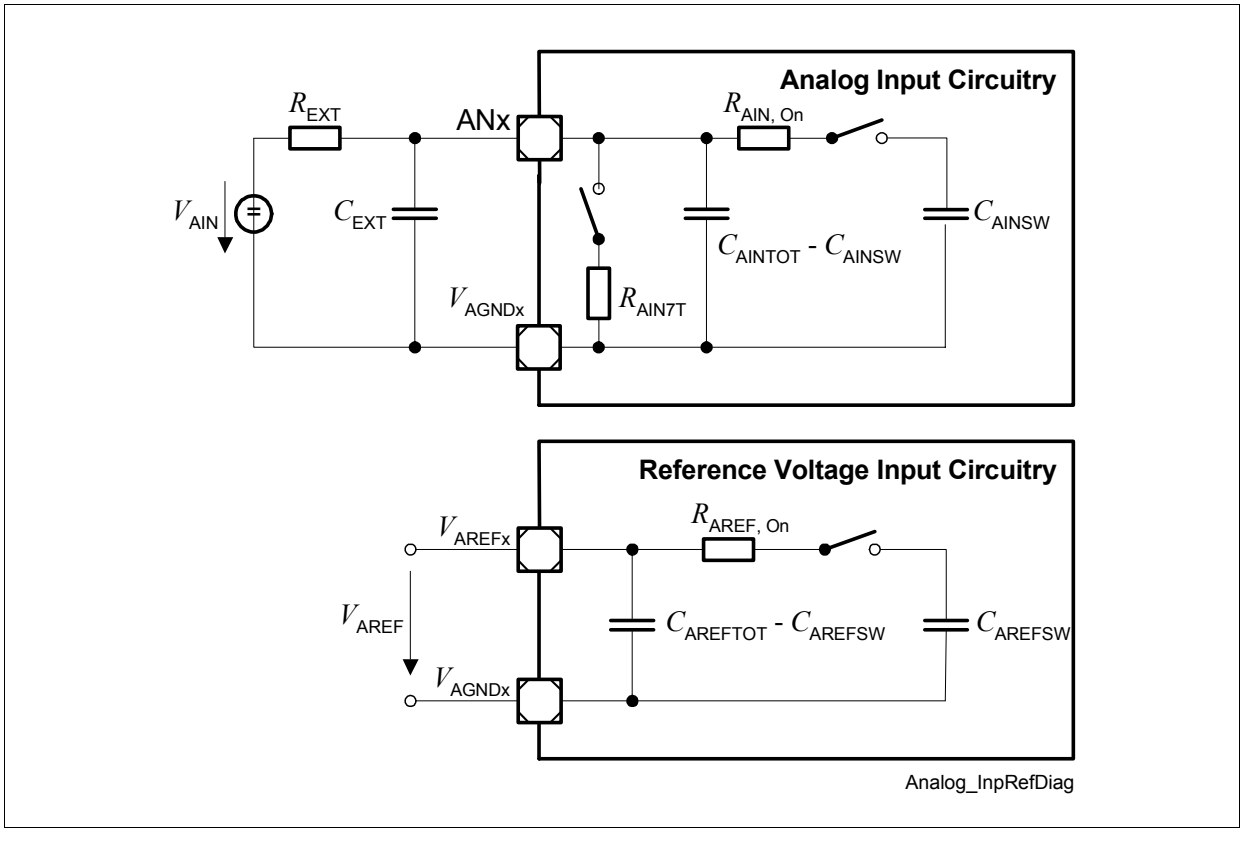


Figure 23 ADC0/ADC1 Input Circuits

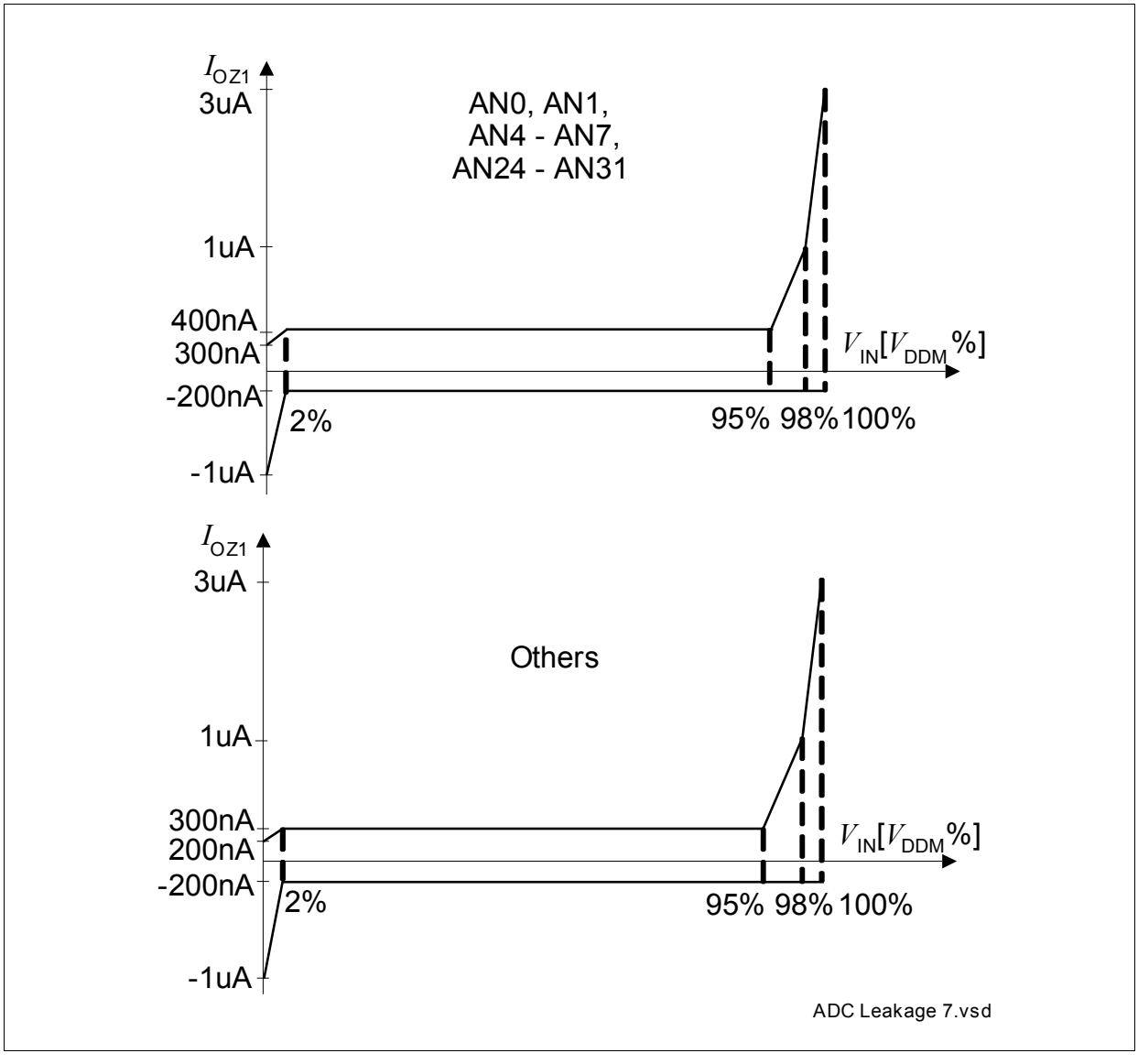


Figure 24 ADC0/ADC1Analog Inputs Leakage

4.2.3 Fast Analog to Digital Converter (FADC)

Table 17 FADC Characteristics (Operating Conditions apply)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
DNL error	E_{DNL}	CC	–	–	±1	LSB	10)
INL error	E_{INL}	CC	–	–	±4	LSB	10)
Gradient error[1)10)]	E_{GRAD}	CC	–	–	±3	%	With calibration, gain 1, 2[2)]
	E_{GRAD}	CC	–	–	±5	%	Without calibration gain 1, 2, 4
	E_{GRAD}	CC	–	–	±6	%	Without calibration gain 8
Offset error[10)]	E_{OFF}[3)]	CC	–	–	±20[4)]	mV	With calibration[2)]
			–	–	±60[4)]	mV	Without calibration
Reference error of internal V_{FAREF}/2	E_{REF}	CC	–	–	±60	mV	–
Analog supply voltages	V_{DDMF}	SR	3.13	–	3.47[5)]	V	–
	V_{DDAF}	SR	1.42	–	1.58[6)]	V	–
Analog ground voltage	V_{SSAF}	SR	-0.1	–	0.1	V	–
Analog reference voltage	V_{FAREF}	SR	3.13	–	3.47[5)7)]	V	Nominal 3.3 V
Analog reference ground	V_{FAGND}	SR	V_{SSAF} - 0.05V	–	V_{SSAF} +0.05V	V	–
Analog input voltage range	V_{AINF}	SR	V_{FAGND}	–	V_{DDMF}	V	–
Analog supply currents	I_{DDMF}	SR	–	–	9	mA	–
	I_{DDAF}	SR	–	–	17	mA	8)
Input current at each V_{FAREF}	I_{FAREF}	CC	–	–	150	µA rms	Independent of conversion
Input leakage current at V_{FAREF} [9)]	I_{FOZ2}	CC	–	–	±500	nA	0 V < V_{IN} < V_{DDMF}
Input leakage current at V_{FAGND}	I_{FOZ3}	CC	–	–	±8	µA	0 V < V_{IN} < V_{DDMF}

Table 17 FADC Characteristics (Operating Conditions apply) (cont'd)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Conversion time	t_C	CC	–	–	21	CLK of f_{ADC}	10-bit conversion
Converter Clock	f_{ADC}	CC	–	–	75	MHz	–
Input resistance of the analog voltage path (Rn, Rp)	R_{FAIN}	CC	100	–	200	kΩ	10)
Channel Amplifier Cutoff Frequency	f_{COFF}	CC	2	–	–	MHz	–
Settling Time of a Channel Amplifier after changing ENN or ENP	t_{SET}	CC	–	–	5	µsec	–

1) Calibration of the gain is possible for the gain of 1 and 2, and not possible for the gain of 4 and 8.
2) Calibration should be performed at each power-up. In case of continuous operation, calibration should be performed minimum once per week.
3) The offset error voltage drifts over the whole temperature range maximum ±3 LSB.
4) Applies when the gain of the channel equals one. For the other gain settings, the offset error increases; it must be multiplied with the applied gain.
5) Voltage overshoot to 4 V are permissible, provided the pulse duration is less than 100 µs and the cumulated summary of the pulses does not exceed 1 h.
6) Voltage overshoot to 1.7 V are permissible, provided the pulse duration is less than 100 µs and the cumulated sum of the pulses does not exceed 1 h.
7) A running conversion may become inexact in case of violating the normal operating conditions (voltage overshoots).
8) Current peaks of up to 40 mA with a duration of max. 2 ns may occur
9) This value applies in power-down mode.
10) Not subject to production test, verified by design / characterization.

The calibration procedure should run after each power-up, when all power supply voltages and the reference voltage have stabilized. The offset calibration must run first, followed by the gain calibration.

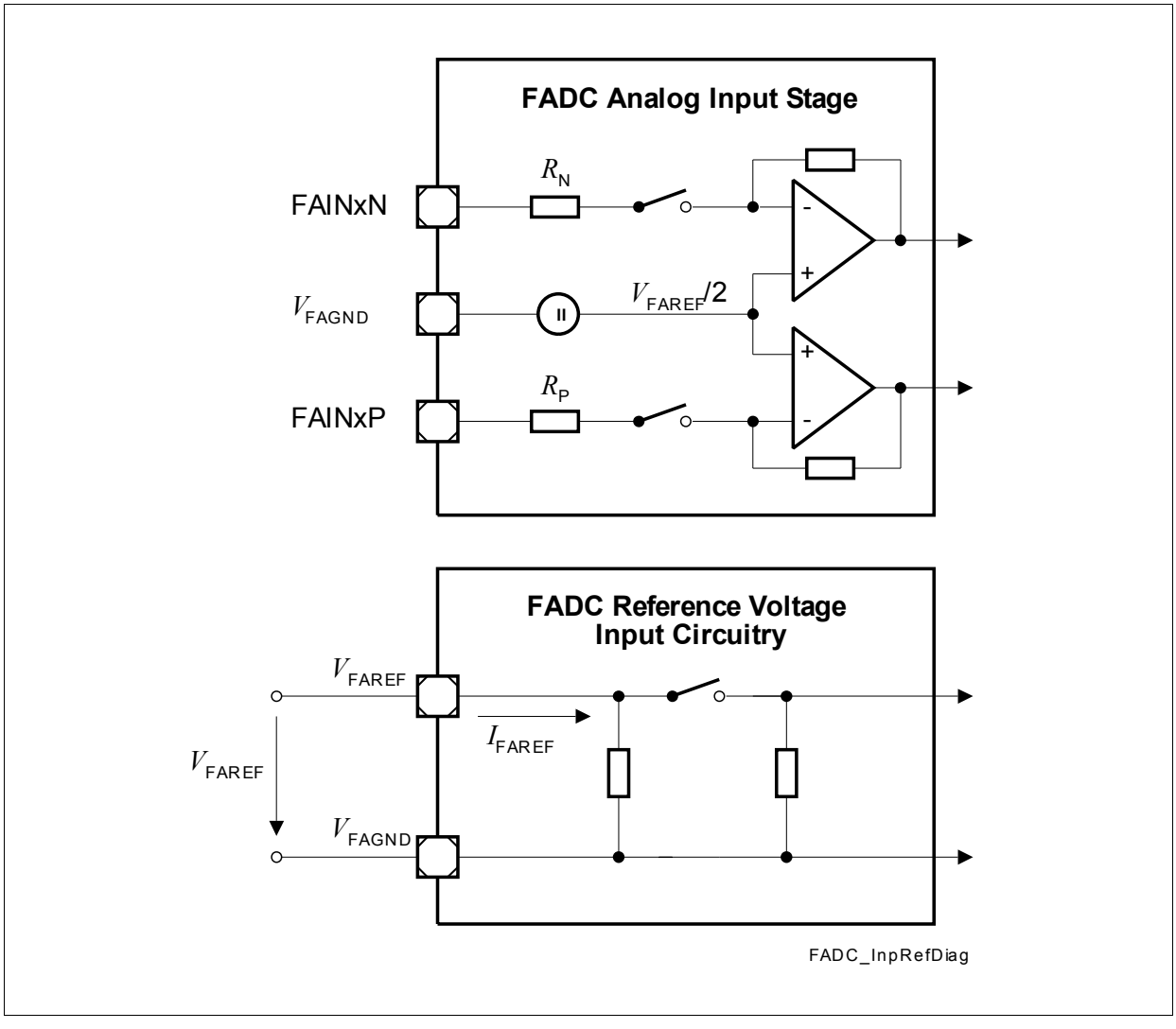


Figure 25 FADC Input Circuits

4.2.4 Oscillator Pins

Table 18 Oscillator Pins Characteristics (Operating Conditions apply)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Frequency Range	f_{OSC}	CC	4	–	25	MHz	–
Input low voltage at XTAL1[1)]	V_{ILX}	SR	-0.2	–	0.3 × V_{DDOSC3}	V	–
Input high voltage at XTAL1[1)]	V_{IHX}	SR	0.7 × V_{DDOSC3}	–	V_{DDOSC3} + 0.2	V	–
Input current at XTAL1	I_{IX1}	CC	–	–	±25	µA	0 V < V_{IN} < V_{DDOSC3}

1) If the XTAL1 pin is driven by a crystal, reaching a minimum amplitude (peak-to-peak) of 0.3 × V_{DDOSC3} is necessary.

Note: It is strongly recommended to measure the oscillation allowance (negative resistance) in the final target system (layout) to determine the optimal parameters for the oscillator operation. Please refer to the limits specified by the crystal supplier.

4.2.5 Temperature Sensor

Table 19 Temperature Sensor Characteristics (Operating Conditions apply)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Temperature Sensor Range	T_{SR}	SR	-40		150	°C	–
Start-up time after resets inactive	t_{TSST}	SR	–	–	10	µs	–
Sensor Inaccuracy	T_{TSA}	CC	–	–	±10	°C	–
A/D Converter clock for DTS signal	f_{ANA}	SR	–	–	10	MHz	conversion with ADC1

Table 20 Temperature Sensor Characteristics (Operating Conditions apply)

Parameter	Symbol		Typical Value	Unit	Note
Temperature of the die at the sensor location	T_{TS}	CC	T_{TS}× = (ADC_Code - 487) 0.396 - 40	°C	10-bit ADC result
			T_{TS}× = (ADC_Code - 1948) 0.099 - 40	°C	12-Bit ADC result

4.2.6 Power Supply Current

"

Table 21 Power Supply Currents (Operating Conditions apply)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
$\overline{\text{PORST}}$ low current at V_{DD}	I_{DD_PORST}	CC	–	–	300	mA	The PLL running at the base frequency
$\overline{\text{PORST}}$ low current at V_{DDP}, and $\overline{\text{PORST}}$ high current without any port activity	I_{DDP_PORST}	CC	–	–	25	mA	The PLL running at the base frequency
Active mode core supply current[1)2)]	I_{DD}	CC	10	–	700	mA	f_{CPU}=150MHzf_{CPU}/f_{SYS} = 2:1
Active mode analog supply current	I_{DDAx}; I_{DDMx}	CC	–	–	–	mA	See ADC0/1 FADC
Stand-by RAM supply current in stand-by	I_{SBSB}	CC	–	–	9	mA	V_{DDSB} = 1V, T_j = 150°C
Oscillator and PLL core power supply	I_{DDOSC}[3)]	CC	–	–	5	mA	–
Oscillator and PLL pads power supply	I_{DDOSC3}	CC	–	–	3.6	mA	–
LVDS port supply (via V_{DDP})[4)]	I_{LVDS}	CC	–	–	50	mA	LVDS pads active
Flash power supply current	I_{DDFL3}	CC	–	–	80	mA	–
Maximum Allowed Power Dissipation[5)]	P_D	SR	–	–	$P_D \times R_{TJA}$ < 25°C	–	worst case T_A = 125°C

1) Infineon Power Loop: CPU and PCP running, all peripherals active. The power consumption of each custom application will most probably be lower than this value, but must be evaluated separately.

2) The I_{DD} decreases for typically 120 mA if the f_{CPU} is decreased for 50 MHz, at constant T_J = 150C, for the Infineon Max Power Loop.
The dependency in this range is, at constant junction temperature, linear.

3) V_{DDOSC} and V_{SSOSC} are not bonded externally in the BC and BD steps of TC1796. An option for bonding them in future steps and products is kept open.

4) In case the LVDS pads are disabled, the power consumption pro pair is negligible (less than 1µA).

5) For the calculation of junction to ambient thermal resistance R_{TJA}, see **Page 130**.

4.3 AC Parameters

All AC parameters are defined with the temperature compensation disabled. That means, keeping the pads constantly at maximum strength.

4.3.1 Testing Waveforms

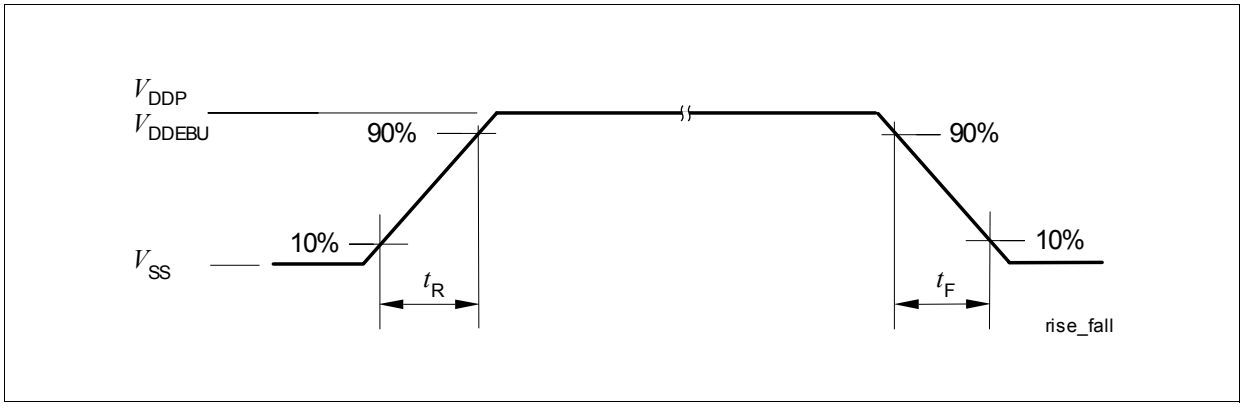


Figure 26 Rise/Fall Time Parameters

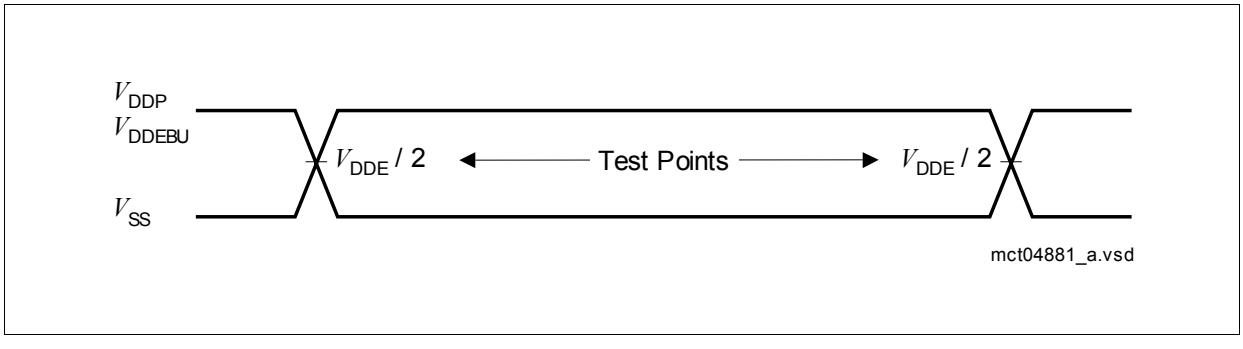


Figure 27 Testing Waveform, Output Delay

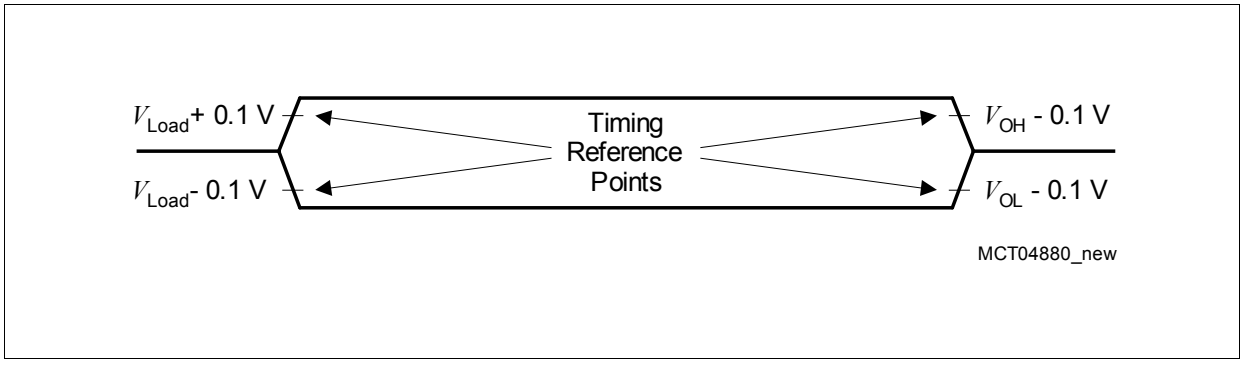


Figure 28 Testing Waveform, Output High Impedance

4.3.2 Output Rise/Fall Times

Table 22 Output Rise/Fall Times (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Class A1 Pads						
Rise/fall times [1]	t_{RA1}, t_{FA1}	–	–	50 140 18000 150 550 65000	ns	Regular (medium) driver, 50 pF Regular (medium) driver, 150 pF Regular (medium) driver, 20 nF Weak driver, 20 pF Weak driver, 150 pF Weak driver, 20 000 pF
Class A2 Pads						
Rise/fall times [1]	t_{RA2}, t_{FA2}	–	–	3.3 6 5.5 16 50 140 18000 150 550 65000	ns	Strong driver, sharp edge, 50 pF Strong driver, sharp edge, 100pF Strong driver, medium edge, 50 pF Strong driver, soft edge, 50 pF Medium driver, 50 pF Medium driver, 150 pF Medium driver, 20 000 pF Weak driver, 20 pF Weak driver, 150 pF Weak driver, 20 000 pF
Class A3 Pads						
Rise/fall times [1]	t_{RA3}, t_{FA3}	–	–	2.5	ns	50 pF
Class A4 Pads						
Rise/fall times [1]	t_{RA3}, t_{FA3}	–	–	2.0	ns	25 pF
Class B Pads						
Rise/fall times [1][2]	t_{RB}, t_{FB}	–	–	3.0 4.0 7.0	ns	35 pF 50 pF 100 pF
Class C Pads						
Rise/fall times	t_{RC}, t_{FC}	–	–	2	ns	–

1) Not all parameters are subject to production test, but verified by design/characterization and test correlation.

2) Parameter test correlation for V_{DDEBU} = 2.5 V ± 5%

4.3.3 Power Sequencing

There is a restriction for the power sequencing of the 3.3 V domain including V_{DDEBU} as shown in **Figure 29**: it must always be higher than 1.5 V domain - 0.5 V. The grey area shows the valid range for $V_{3.3V}$ and V_{DDEBU} relative to an exemplary 1.5 V ramp.
V_{DDP}, V_{DDOSC3}, V_{DDFL3}, V_{DDM}, V_{DDMF} belong to the 3.3 V power supply domain, that is referenced in **Figure 29** as $V_{3.3}$. The V_{DDM} and V_{DDMF} sub domains are connected with anti parallel ESD protection diodes in TC1796 design steps BC and BD. The V_{DDM}, V_{DDMF}, V_{DDP}, V_{DDOSC3} sub domains are connected with anti parallel ESD protection diodes in TC1796 design step BE.
V_{DD}, V_{DDOSC} and V_{DDAF} belong to the 1.5 V power supply domain, referenced as $V_{1.5}$.
V_{DDEBU} belongs to its own 2.5V to 3.3V domain.

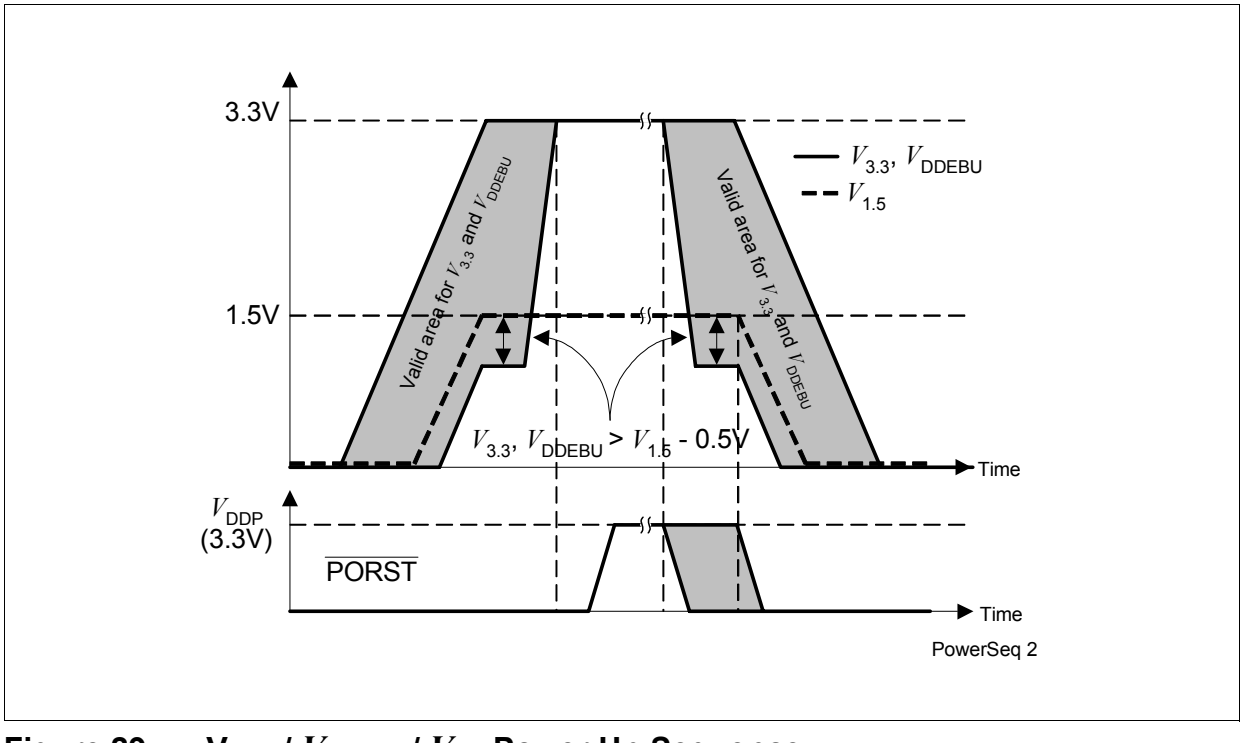


Figure 29 V_{DDP} / V_{DDEBU} / V_{DD} Power Up Sequence

All ground pins V_{SS} must be externally connected to one single star point in the system. The difference voltage between the ground pins must not exceed 200 mV.

The $\overline{\text{PORST}}$ signal must be activated at latest before any power supply voltage falls below the levels shown on the figure below. In this case, only the memory row of a Flash memory that was a target of a write at the moment of the power loss will contain unreliable content. Additionally, the $\overline{\text{PORST}}$ signal should be activated as soon as possible. The sooner the $\overline{\text{PORST}}$ signal is activated, the less time the system operates outside of the normal operating power supply range.

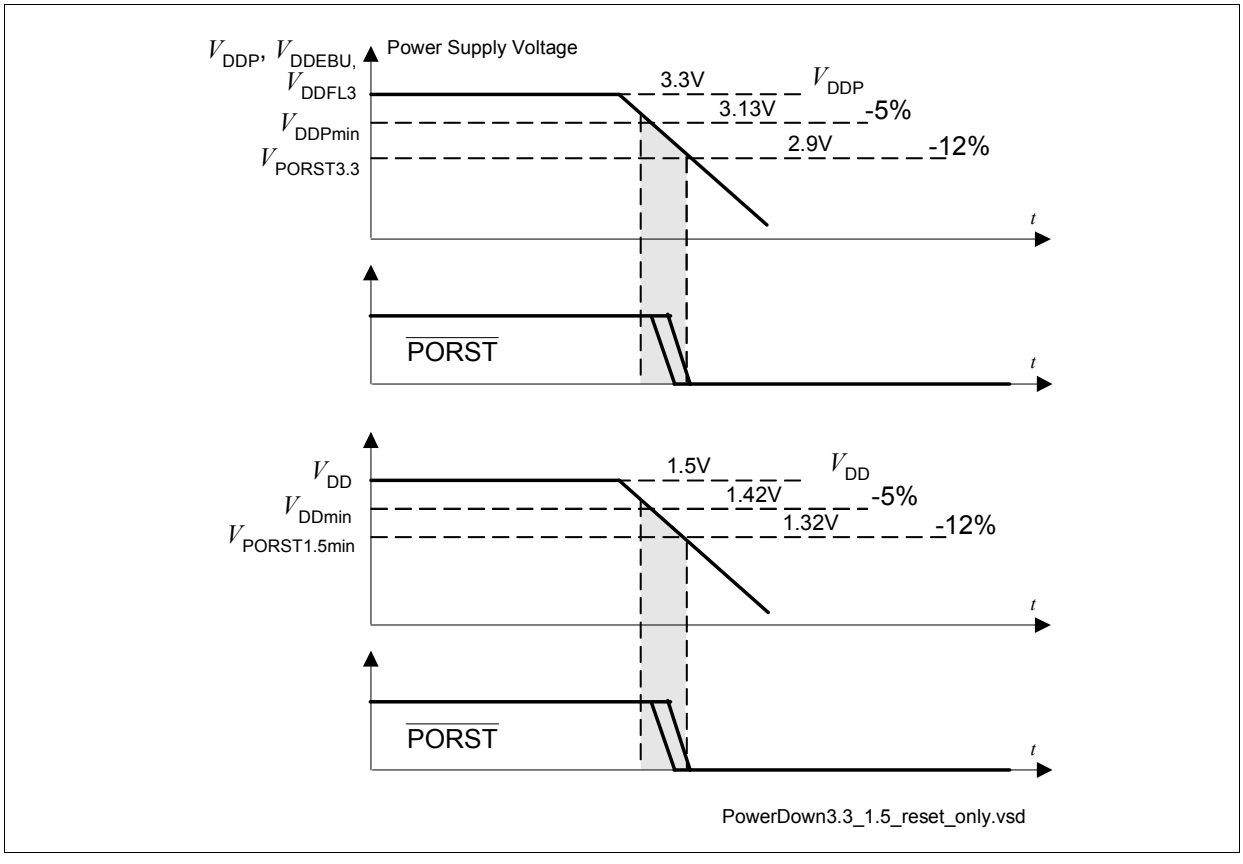


Figure 30 Power Down / Power Loss Sequence

4.3.4 Power, Pad and Reset Timing

Table 23 Power, Pad and Reset Timing Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Min. V_{DDP} voltage to ensure defined pad states[1]	V_{DDPPA}	CC	0.6	–	–	V	–
Oscillator start-up time[2]	t_{OSCS}	CC	–	–	10	ms	–
Minimum $\overline{\text{PORST}}$ active time after power supplies are stable at operating levels	t_{POA}	SR	10	–	–	ms	–
$\overline{\text{HDRST}}$ pulse width	t_{HD}	CC	1024 clock cycles[3][6]	–	–	f_{SYS}	–
$\overline{\text{PORST}}$ rise time	t_{POR}	SR	–	–	50	ms	–
Setup time to $\overline{\text{PORST}}$ rising edge[4]	t_{POS}	SR	0	–	–	ns	–
Hold time from $\overline{\text{PORST}}$ rising edge[4]	t_{POH}	SR	100	–	–	ns	–
Setup time to $\overline{\text{HDRST}}$ rising edge[5]	t_{HDS}	SR	0	–	–	ns	–
Hold time from $\overline{\text{HDRST}}$ rising edge[5]	t_{HDH}	SR	100 + (2 × 1/ f_{SYS})[6]	–	–	ns	–
Ports inactive after $\overline{\text{PORST}}$ reset active[7][8]	t_{PIP}	CC	–	–	150	ns	–
Ports inactive after $\overline{\text{HDRST}}$ reset active	t_{PI}	CC	–	–	150 + 5 × 1/ f_{SYS}	ns	–
Minimum V_{DDP} $\overline{\text{PORST}}$ activation threshold[9]	$V_{PORST3.3}$	SR	–	–	2.9	V	–
Minimum V_{DD} $\overline{\text{PORST}}$ activation threshold[9]	$V_{PORST1.5}$	SR	–	–	1.32	V	–
Power on Reset Boot Time[9]	t_{BP}	CC	–	–	2	ms	–
Hardware/Software Reset Boot Time at f_{CPU}=150MHz[10]	t_B	CC	150	–	350	µs	–

1) This parameter is valid under assumption that $\overline{\text{PORST}}$ signal is constantly at low level during the power-up/power-down of the V_{DDP}.
2) t_{OSCS} is defined from the moment when V_{DDOSC3} = 3.13V until the oscillations reach an amplitude at XTAL1 of 0,3*V_{DDOSC3}. This parameter is verified by device characterization. The external oscillator circuitry must be optimized by the customer and checked for negative resistance as recommended and specified by crystal suppliers.
3) Any $\overline{\text{HDRST}}$ activation is internally prolonged to 1024 FPI bus clock (f_{SYS}) cycles.
4) Applicable for input pins $\overline{\text{TESTMODE}}$, $\overline{\text{TRST}}$, $\overline{\text{BRKIN}}$, and TXD1A with noise suppression filter of $\overline{\text{PORST}}$ switched-on (BYPASS = 0).
5) The setup/hold values are applicable for Port 0 and Port 10 input pins with noise suppression filter of $\overline{\text{HDRST}}$ switched-on (BYPASS = 0), independently whether $\overline{\text{HDRST}}$ is used as input or output.
6) f_{SYS} = f_{CPU}/2
7) Not subject to production test, verified by design / characterization.
8) This parameter includes the delay of the analog spike filter in the $\overline{\text{PORST}}$ pad.
9) The duration of the boot-time is defined between the rising edge of the $\overline{\text{PORST}}$ and the moment when the first user instruction has entered the CPU and its processing starts.
10) The duration of the boot time is defined between the following events:
    1. Hardware reset: the falling edge of a short $\overline{\text{HDRST}}$ pulse and the moment when the first user instruction has entered the CPU and its processing starts, if the $\overline{\text{HDRST}}$ pulse is shorter than 1024 × T_{SYS}.
    If the $\overline{\text{HDRST}}$ pulse is longer than 1024 × T_{SYS}, only the time beyond the 1024 × T_{SYS} should be added to the boot time ($\overline{\text{HDRST}}$ falling edge to first user instruction).
    2. Software reset: the moment of starting the software reset and the moment when the first user instruction has entered the CPU and its processing starts

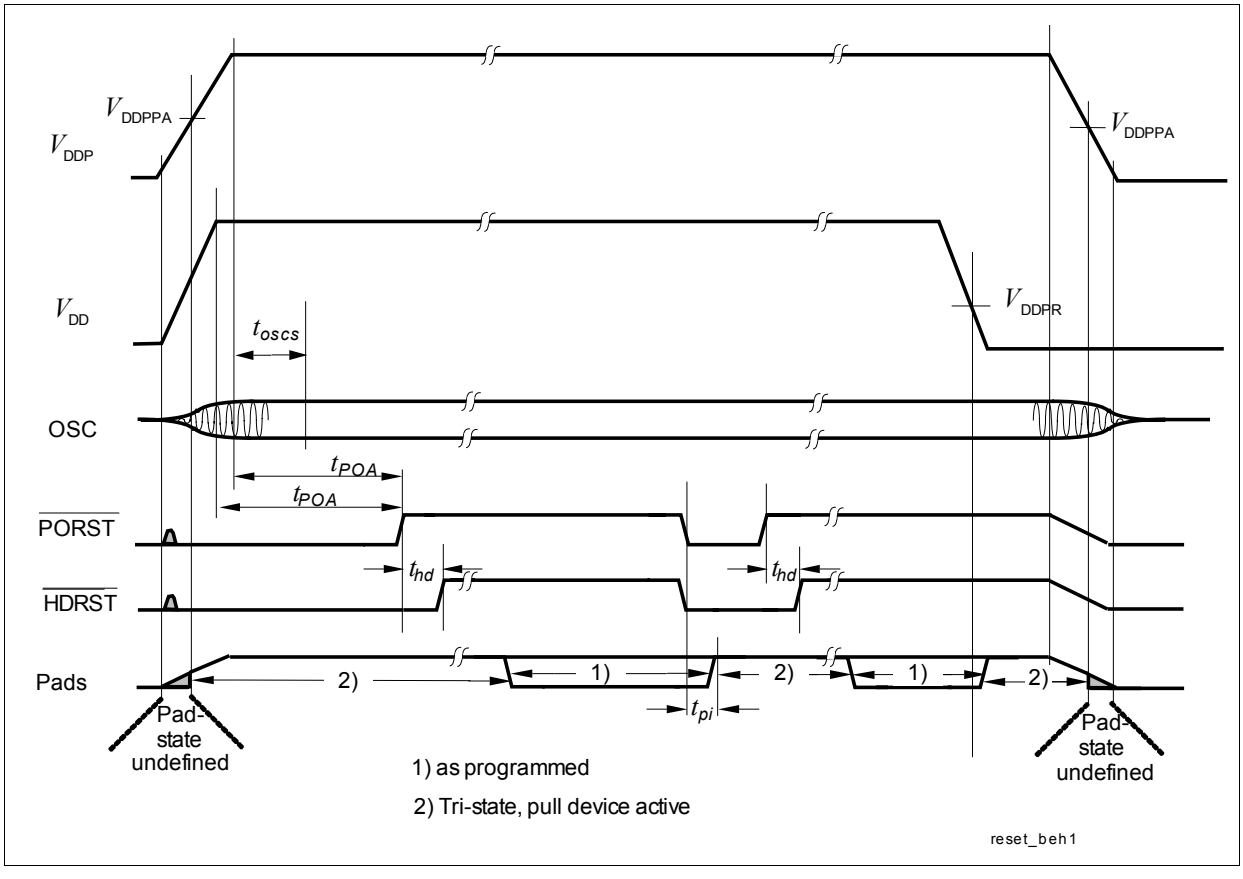


Figure 31 Power, Pad and Reset Timing

4.3.5 Phase Locked Loop (PLL)

Note: All PLL characteristics defined on this and the next page are verified by design characterization.

Table 24 PLL Parameters (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Accumulated jitter	D_P	See Figure 32	–	–	–	–
VCO frequency range	f_{VCO}	400	–	500	MHz	–
		600	–	700	MHz	–
		500	–	600	MHz	–
PLL base frequency[1)]	$f_{PLLBASE}$	140	–	320	MHz	–
		150	–	400	MHz	–
		200	–	480	MHz	–
PLL lock-in time	t_L	–	–	200	µs	–

1) The CPU base frequency which is selected after reset is calculated by dividing the limit values by 16 (this is the K factor after reset).

Phase Locked Loop Operation

When PLL operation is enabled and configured, the PLL clock f_{VCO} (and with it the CPU clock f_{CPU}) is constantly adjusted to the selected frequency. The relation between f_{VCO} and f_{SYS} is defined by: $f_{VCO} = K \times f_{CPU}$. The PLL causes a jitter of f_{CPU} and affects the clock outputs BFCLKO, TRCLK, and SYSCLK (P1.12) which are derived from the PLL clock f_{VCO}.

There will be defined two formulas that define the (absolute) approximate maximum value of jitter D_P in ns dependent on the K-factor, the CPU clock frequency f_{CPU} in MHz, and the number P of consecutive f_{CPU} clock periods.

$$P \times K < 385 \qquad Dp[ns] = \frac{7000 \times P}{fcpu^2[MHz] \times K} + 0,535 \tag{1}$$

$$P \times K \geq 385 \qquad Dp[ns] = \frac{2700000}{fcpu^2[MHz] \times K^2} + 0,535 \tag{2}$$

Note: The frequency of system clock f_{SYS} can be selected to be either f_{CPU} or $f_{CPU}/2$.

With rising number P of clock cycles the maximum jitter increases linearly up to a value of P that is defined by the K-factor of the PLL. Beyond this value of P the maximum accumulated jitter remains at a constant value. Further, a lower CPU clock frequency f_{CPU} results in a higher absolute maximum jitter value.

Figure 32 gives the jitter curves for several K/f_{CPU} combinations.

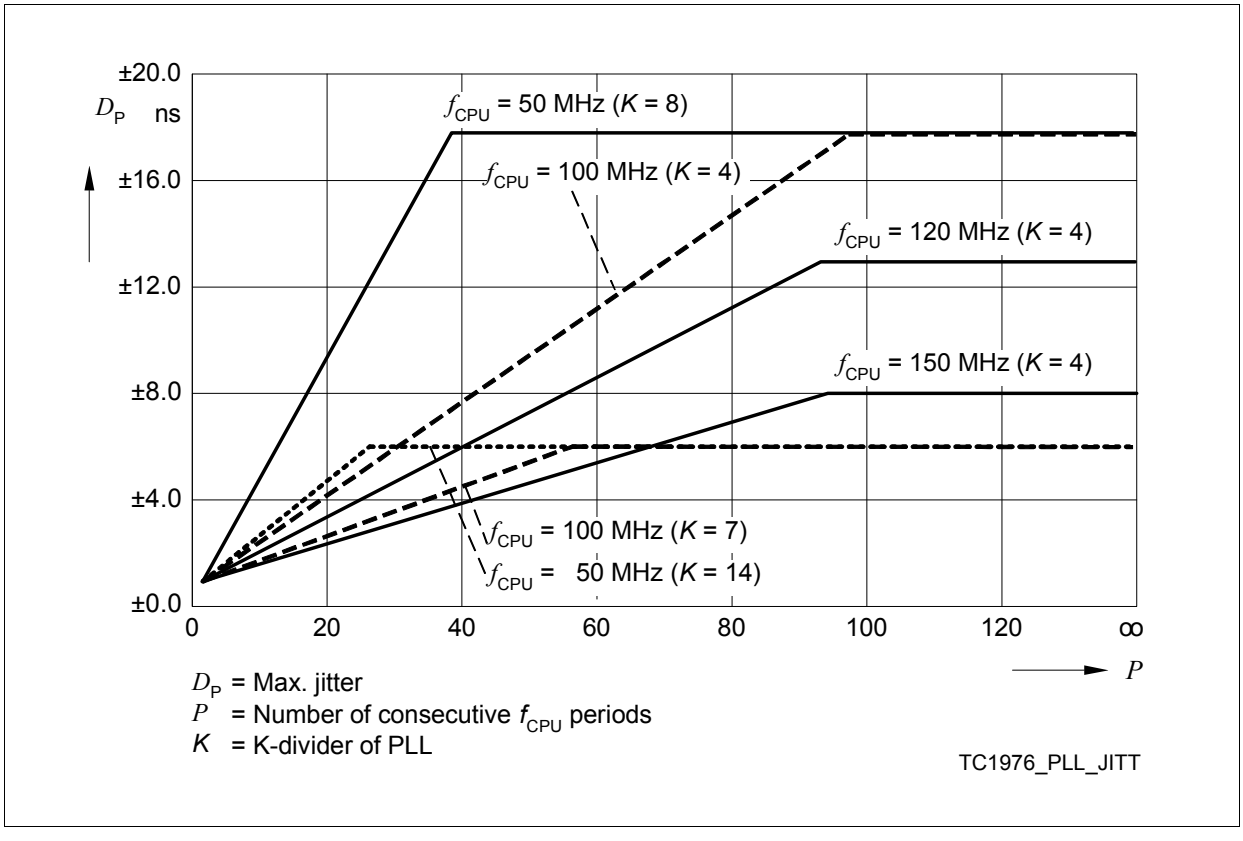


Figure 32 Approximated Maximum Accumulated PLL Jitter for Typical CPU Clock Frequencies f_{CPU} (overview)

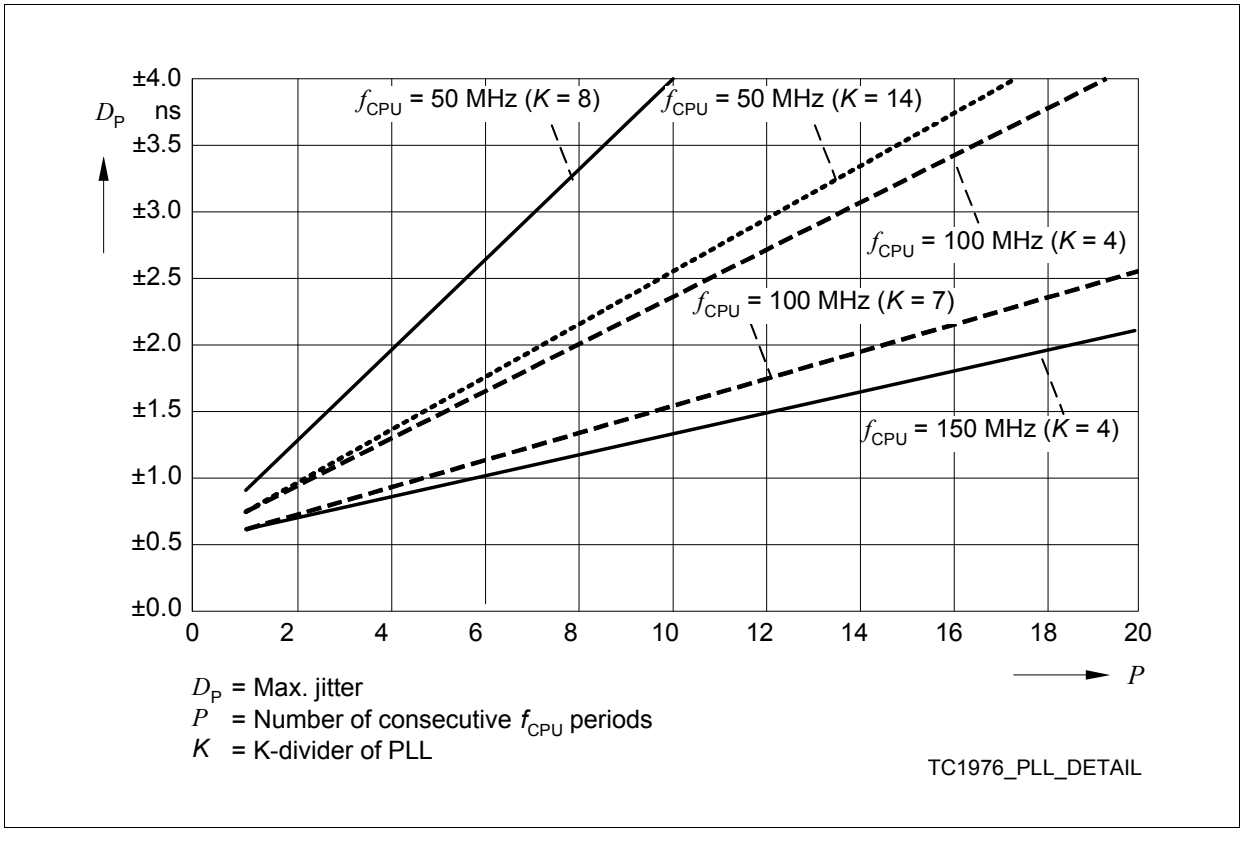


Figure 33 Approximated Maximum Accumulated PLL Jitter for Typical CPU Clock Frequencies f_{CPU} (detail)

Note: The specified PLL jitter values are valid if the capacitive load at the External Bus Unit (EBU) is limited to C_L=20pF.

Note: The maximum peak-to-peak noise on the Core Supply Voltage (measured between V_{DD} at pin E23 and V_{SS} at pin D23, or adjacent supply pairs) is limited to a peak-to-peak voltage of V_{PP} = 30mV. This condition can be achieved by appropriate blocking of the Core Supply Voltage as near as possible to the supply pins and using PCB supply and ground planes.=20pF.

4.3.6 BFCLKO Output Clock Timing

V_{SS} = 0 V;V_{DD} = 1.5 V ± 5%; V_{DDEBU} = 2.5 V ± 5% and 3.3 V ± 5%;
T_A = -40 °C to +125 °C; C_L = 35 pF

Table 25 BFCLK0 Output Clock Timing Parameters[1)]

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
BFCLKO clock period	t_{BFCLKO}	CC	13.33[2)]	–	–	ns	–
BFCLKO high time	t_5	CC	3	–	–	ns	–
BFCLKO low time	t_6	CC	3	–	–	ns	–
BFCLKO rise time	t_7	CC	–	–	3	ns	–
BFCLKO fall time	t_8	CC	–	–	3	ns	–
BFCLKO duty cycle $t_5/(t_5 + t_6)$[3)]	$DC24$	CC	45	50	55	%	divider of 2, 4, ...[4)]
BFCLKO duty cycle $t_5/(t_5 + t_6)$[3)]	$DC3$	CC	30	33.33	36	%	divider of 3 [4)]
BFCLKO high time reduction[5)]	dt_5	CC	–	–	1.1	ns	C_L = 20pF

1) Not subject to production test, verified by design/characterization.
2) The PLL jitter characteristics add to this value according to the application settings. See the PLL jitter parameters.
3) The PLL jitter is not included in this parameter. If the BFCLKO frequency is equal to f_{CPU}, the K-divider setting determines the duty cycle.
4) The division ratio between LMB and BFCLKO frequency is set by EBU_BFCON.EXTCLOCK.
5) Due to asymmetry of the delays and slopes of the rising and falling edge of the pad. The influence of the PLL jitter is included in this parameter. This parameter should be applied taking the typical value of the duty cycle in the account, not the minimum or maximum value.

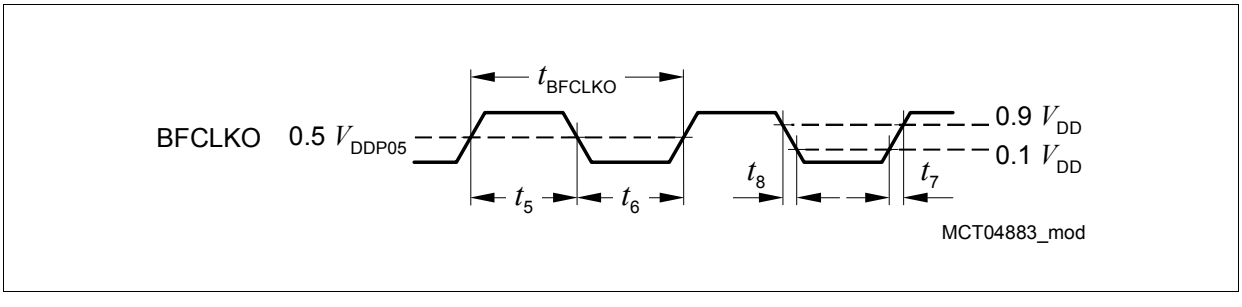


Figure 34 BFCLKO Output Clock Timing

BFCLK Timing and PLL Jitter

The BFCLK timing is important for calculating the timing of an external flash memory. In principle BFCLK timing can be derived from the PLL jitter formulas. In case of only EBU synchronous read access to the flash device the worst case jitter is partially lower.

For one BFCLK with a cycle time of 13,33 ns the maximum jitter is
t_{JPP} = |+/-620 ps|
For two BFCLKs with an accumulated cycle time of 26,66 ns the maximum jitter is
t_{JPACC} = |+/- 660 ps|

4.3.7 Debug Trace Timing

V_{SS} = 0 V; V_{DDP} = 3.13 to 3.47 V (Class A); T_A = -40 °C to +125 °C;
C_L (TRCLK) = 25 pF; C_L (TR[15:0]) = 50 pF;

Table 26 Debug Trace Timing Parameter[1)]

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
TR[15:0] new state from TRCLK rising edge	t_9	CC	-1	–	4	ns	–

1) Not subject to production test, verified by design/characterization.

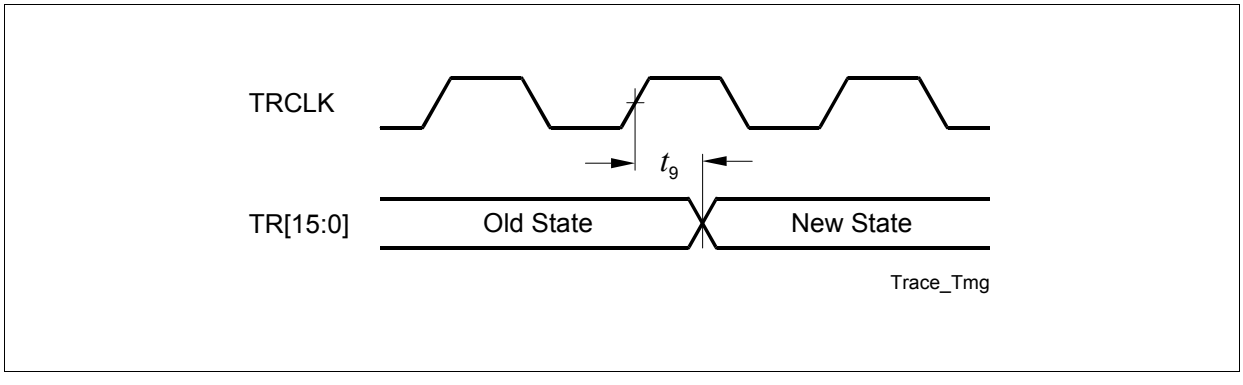


Figure 35 Debug Trace Timing

4.3.8 JTAG Interface Timing

Operating Conditions apply, CL = 50 pF

Table 27 TCK Clock Timing Parameter

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
TCK clock period[1)]	t_{TCK}	SR	25	–	–	ns	–
TCK high time	t_1	SR	10	–	–	ns	–
TCK low time	t_2	SR	10	–	–	ns	–
TCK clock rise time	t_3	SR	–	–	4	ns	–
TCK clock fall time	t_4	SR	–	–	4	ns	–

1) f_{TCK} should be lower or equal to f_{SYS}.

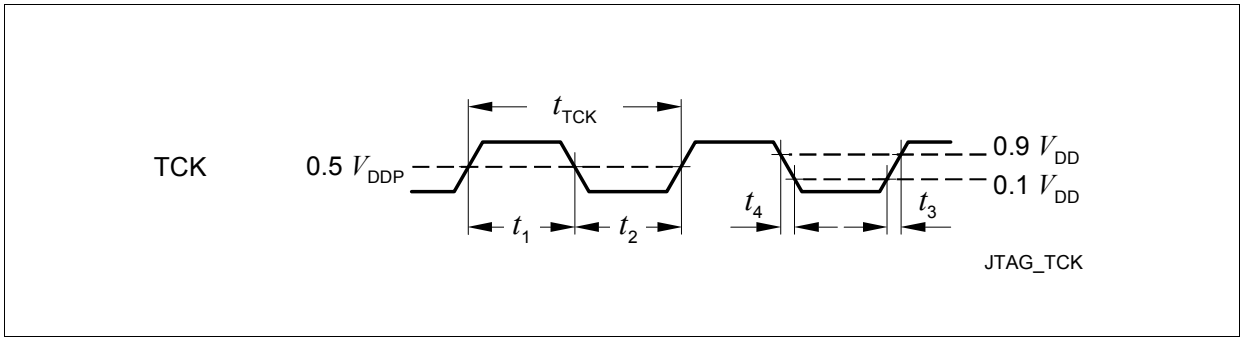


Figure 36 TCK Clock Timing

Table 28 JTAG Timing Parameters[1)]

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
TMS setup to TCK rising edge	t_1	SR	6.0	–	–	ns	–
TMS hold to TCK rising edge	t_2	SR	6.0	–	–	ns	–
TDI setup to TCK rising edge	t_1	SR	6.0	–	–	ns	–
TDI hold to TCK rising edge	t_2	SR	6.0	–	–	ns	–
TDO valid output from TCK falling edge[2)]	t_3	CC	–	–	13	ns	C_L = 50 pF
	t_3	CC	3.0	–	–	ns	C_L = 20 pF
TDO high impedance to valid output from TCK falling edge[2)]	t_4	CC	–	–	14	ns	C_L = 50 pF
TDO valid output to high impedance from TCK falling edge[2)]	t_5	CC	–	–	13.5	ns	C_L = 50 pF

1) f_{TCK} should be lower or equal to f_{SYS}.

2) The falling edge on TCK is used to capture the TDO timing.

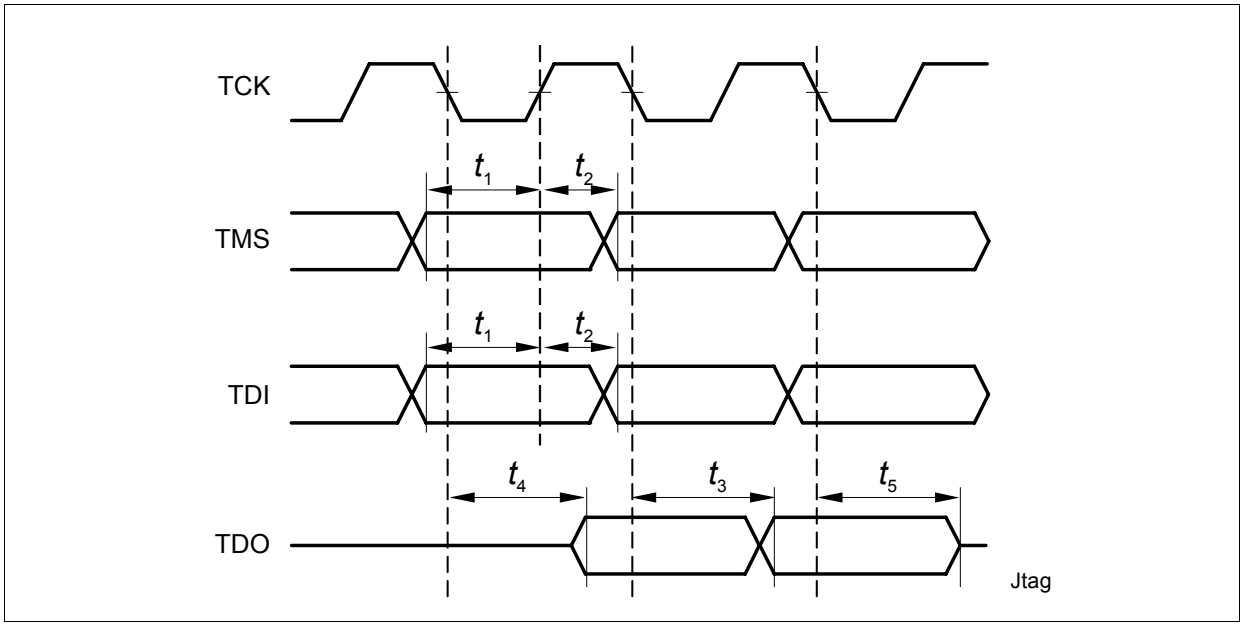


Figure 37 JTAG Timing

*Note: The JTAG module is fully compliant with IEEE1149.1-2000 with JTAG clock at 20 MHz. The JTAG clock at 40MHz is possible with the modified timing diagram shown in **Figure 37**.*

4.3.9 EBU Demultiplexed Timing

V_{SS} = 0 V;V_{DD} = 1.5 V ± 5%; V_{DDEBU} = 2.5 V ± 5% and 3.3 V ± 5%, Class B pins;
T_A = -40 °C to +125 °C; C_L = 35 pF;

Table 29 EBU Demultiplexed Timing Parameters[1)]

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Output delay from BFCLKO rising edge[2)]	t_{10}	CC	0	–	5	ns	–
$\overline{RD}$ active/inactive after BFCLKO rising edge[2)]	t_{12}	CC	0	–	3	ns	–
Data setup to BFCLKO rising edge[2)]	t_{13}	SR	8.5	–	–	ns	–
Data hold from BFCLKO rising edge[2)]	t_{14}	SR	0	–	–	ns	–
$\overline{WAIT}$ setup (low or high) to BFCLKO rising edge[2)]	t_{15}	SR	3	–	–	ns	–
$\overline{WAIT}$ hold (low or high) from BFCLKO rising edge[2)]	t_{16}	SR	2	–	–	ns	–
Data hold after RD/$\overline{WR}$ rising edge	t_{17}	SR	0	–	–	ns	–

1) Not subject to production test, verified by design/characterization.

2) Valid for BFCON.EXTCLOCK = 00_B.

4.3.9.1 Demultiplexed Read Timing

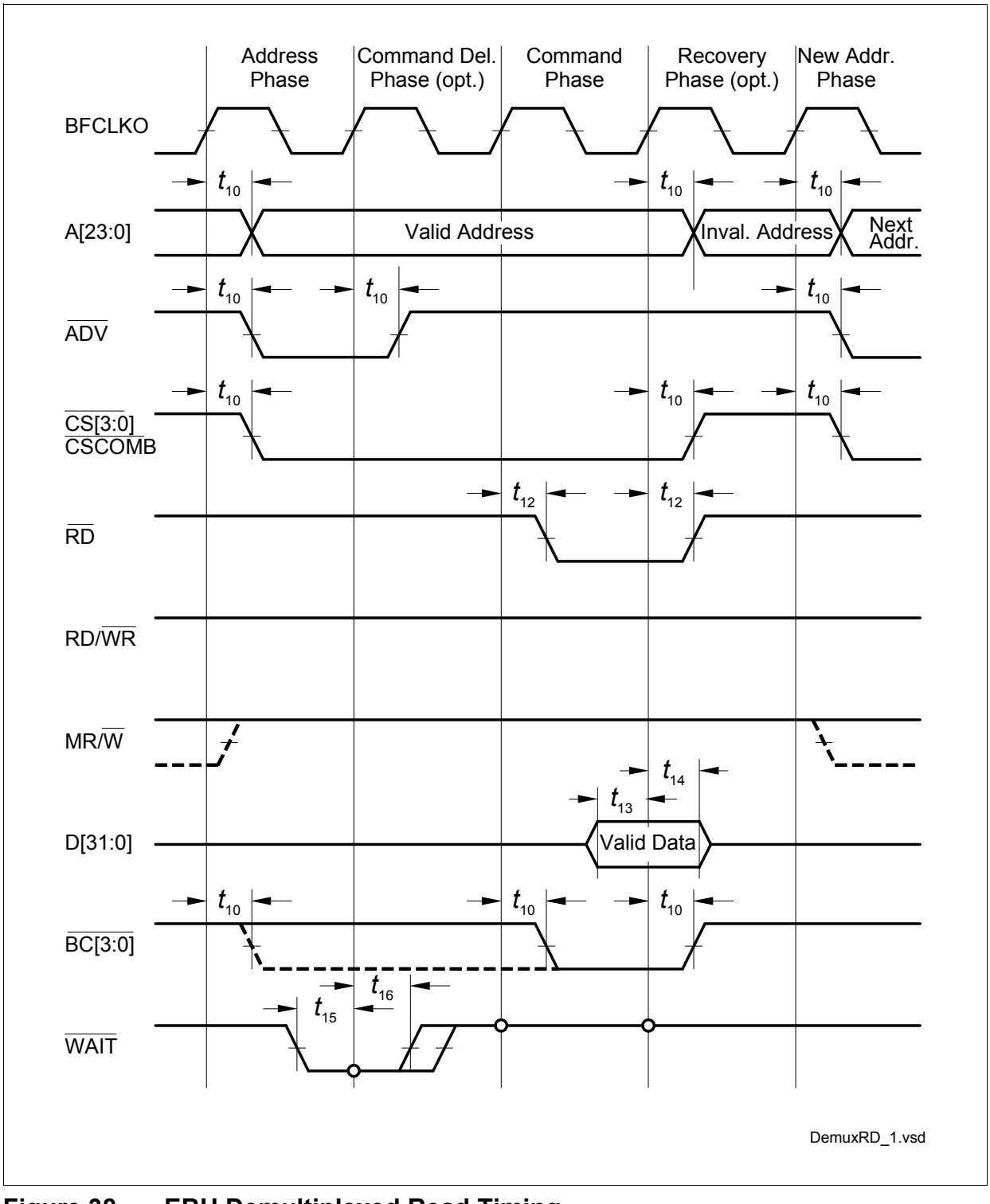


Figure 38 EBU Demultiplexed Read Timing

4.3.9.2 Demultiplexed Write Timing

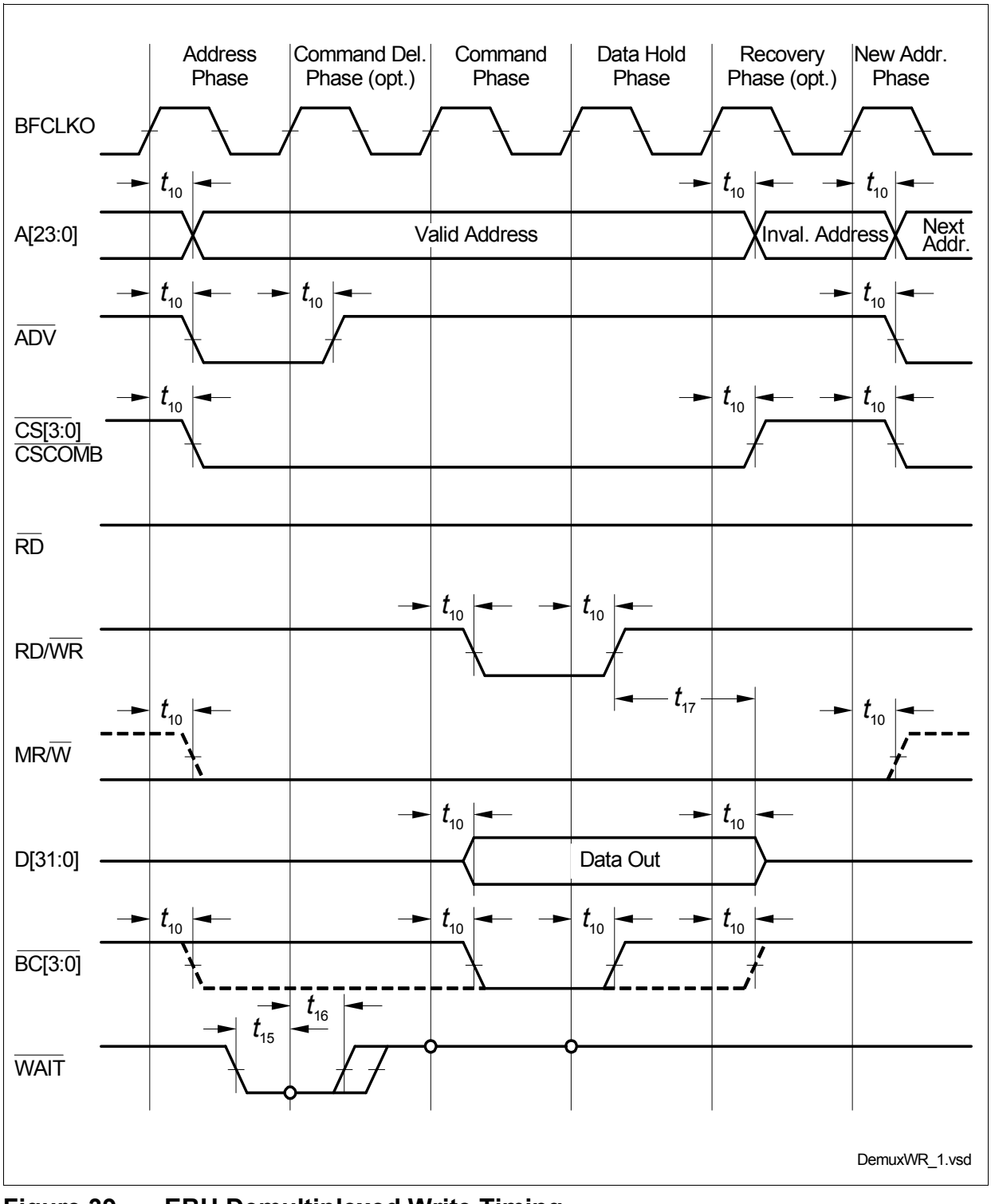


Figure 39 EBU Demultiplexed Write Timing

4.3.10 EBU Burst Mode Read Timing

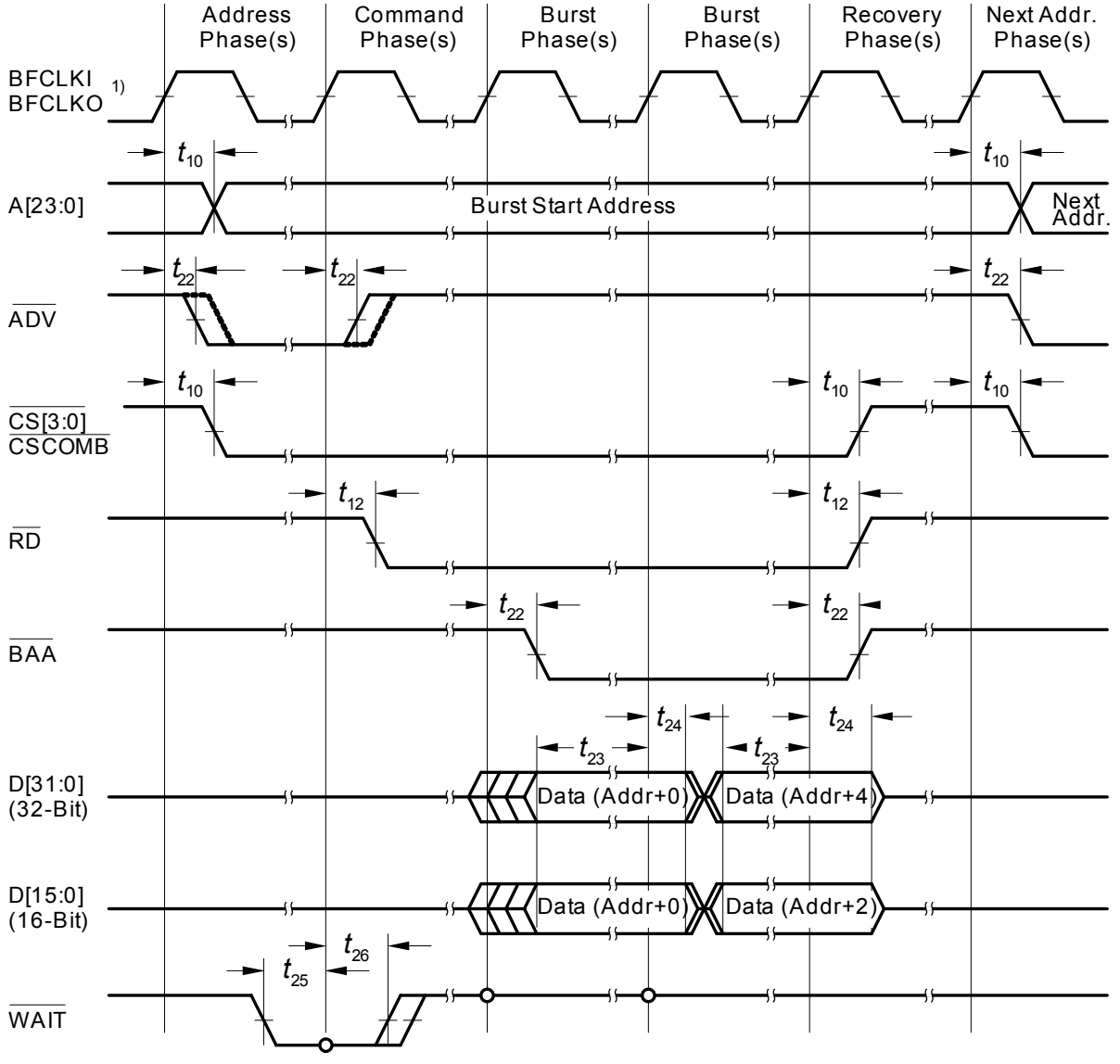
V_{SS} = 0 V;V_{DD} = 1.5 V ± 5%; V_{DDEBU} = 2.5 V ± 5% and 3.3 V ± 5%, Class B pins;
T_A = -40 °C to +125 °C; C_L = 35 pF;

Table 30 EBU Burst Mode Read Timing Parameters[1)]

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Output delay from BFCLKO rising edge	t_{10}	CC	0	–	5	ns	–
$\overline{RD}$ active/inactive after BFCLKO rising edge	t_{12}	CC	0	–	5	ns	–
$\overline{CS}$x output delay from BFCLKO rising edge	t_{21}	CC	0	–	4	ns	–
$\overline{ADV}$/$\overline{BAA}$ active/inactive after BFCLKO rising edge[2)]	t_{22}	CC	0	–	4	ns	–
Data setup to BFCLKI rising edge	t_{23}	SR	3	–	–	ns	–
Data hold from BFCLKI rising edge	t_{24}	SR	0	–	–	ns	–
$\overline{WAIT}$ setup (low or high) to BFCLKI rising edge	t_{25}	SR	3	–	–	ns	–
$\overline{WAIT}$ hold (low or high) from BFCLKI rising edge	t_{26}	SR	2	–	–	ns	–

1) Not subject to production test, verified by design/characterization.

2) This parameter is valid for BFCON.EBSE0 = 1 (or BFCON.EBSE1 = 1). Note that t_{22} is increased by: 1/2 of the LMB bus clock period $T_{CPU} = 1/f_{CPU}$ when BFCON.EBSE0 = 0 (or BFCON.EBSE1 = 0).



1) Output delays are always referenced to BCLKO. The reference clock for input characteristics depends on bit EBU_BFCON.FDBKEN.
EBU_BFCON.FDBKEN = 0:BFCLKO is the input reference clock.
EBU_BFCON.FDBKEN = 1:BFCLKI is the input reference clock (EBU clock feedback enabled).

BurstRD_4.vsd

Figure 40 EBU Burst Mode Read Timing

4.3.11 EBU Arbitration Signal Timing

V_{SS} = 0 V;V_{DD} = 1.5 V ± 5%; V_{DDEBU} = 2.5 V ± 5% and 3.3 V ± 5%, Class B pins;
T_A = -40°C to +125 °C; C_L = 35 pF;

Table 31 EBU Arbitration Signal Timing Parameters[1)]

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Output delay from CLKOUT rising edge	t_{27}	CC	–	–	3	ns	–
Data setup to CLKOUT falling edge	t_{28}	SR	8	–	–	ns	–
Data hold from CLKOUT falling edge	t_{29}	SR	2	–	–	ns	–

1) Not subject to production test, verified by design/characterization.

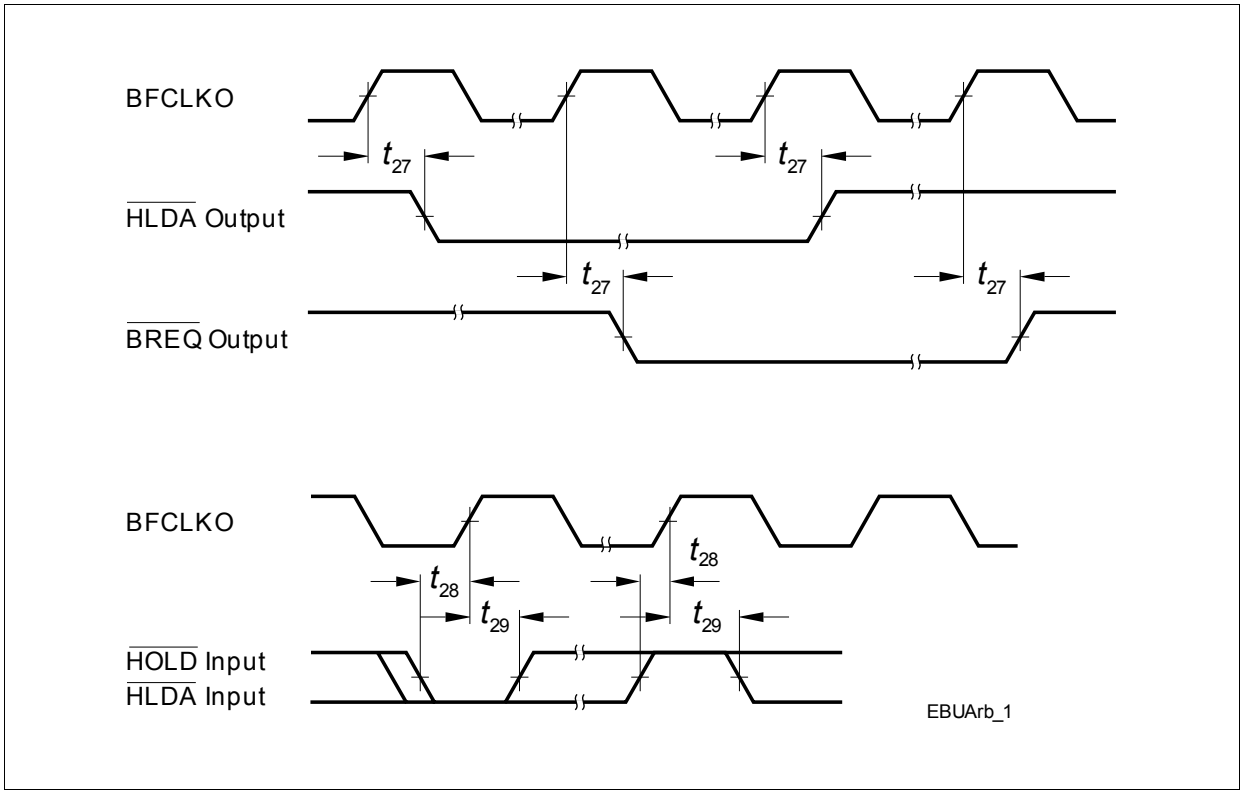


Figure 41 EBU Arbitration Signal Timing

4.3.12 Peripheral Timings

Note: Peripheral timing parameters are not subject to production test. They are verified by design/characterization.

4.3.12.1 Micro Link Interface (MLI) Timing

Table 32 MLI Timing Parameters (Operating Conditions apply), C_L = 50 pF

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
TCLK clock period[1)2)]	t_{30}	CC	2[3)]	–	–	1 / f_{SYS}	–
RCLK clock period	t_{31}	SR	1	–	–	1 / f_{SYS}	–
MLI outputs delay from TCLK rising edge	t_{35}	CC	0	–	8	ns	–
MLI inputs setup to RCLK falling edge	t_{36}	SR	4	–	–	ns	–
MLI inputs hold to RCLK falling edge	t_{37}	SR	4	–	–	ns	–
RREADY output delay from RCLK falling edge	t_{38}	CC	0	–	8	ns	–

1) TCLK signal rise/fall times are the same as the A2 Pads rise/fall times.

2) TCLK high and low times can be minimum 1 × $T_{MLI.}$

3) When f_{SYS} = 75 MHz, t_{30} = 26,67ns

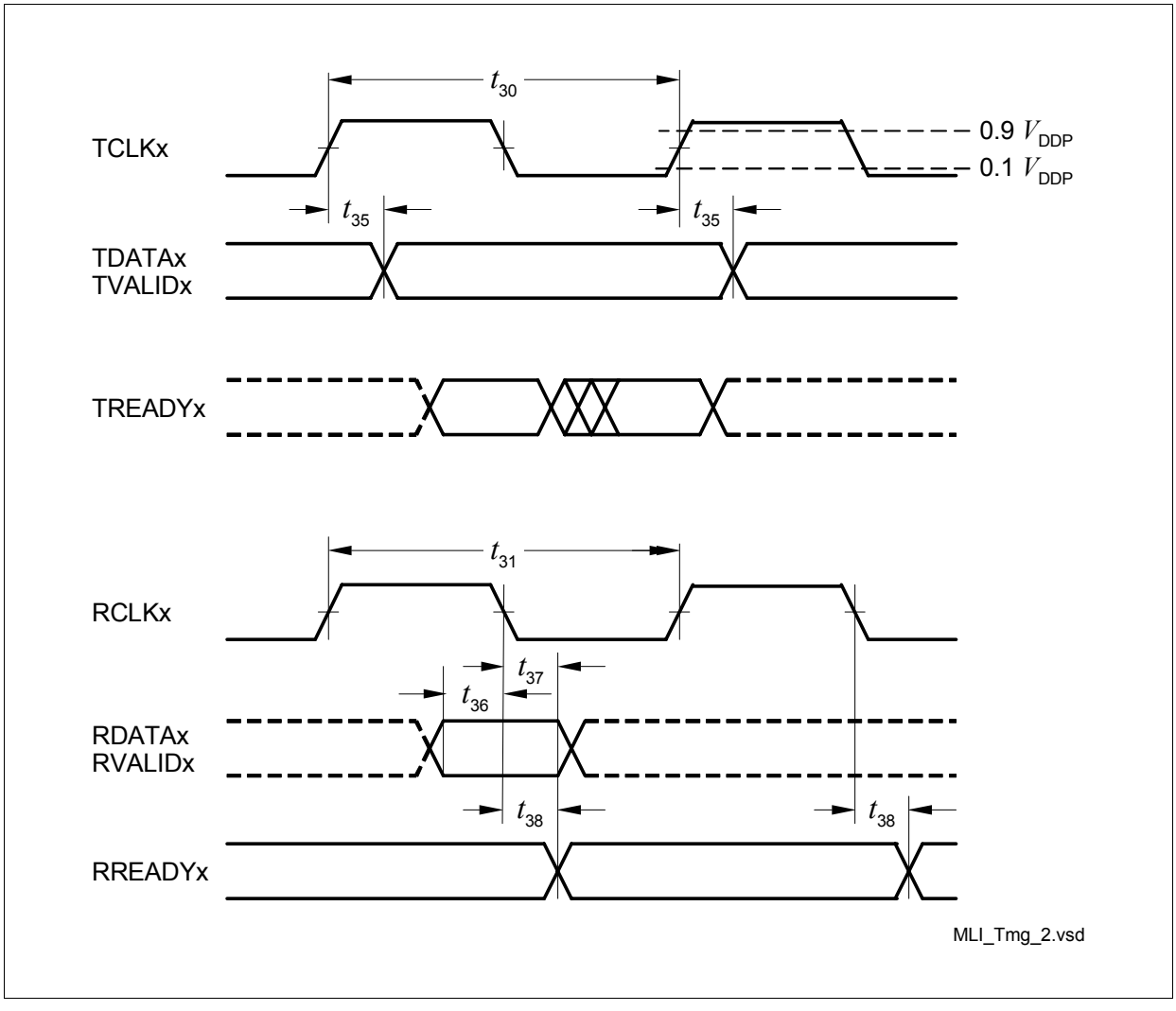


Figure 42 MLI Interface Timing

Note: The generation of RREADYx is in the input clock domain of the receiver. The reception of TREADYx is asynchronous to TCLKx.

4.3.12.2 Micro Second Channel (MSC) Interface Timing

Table 33 MSC Interface Timing (Operating Conditions apply), C_L = 50 pF

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
FCLP clock period[1)2)]	t_{40}	CC	2 × T_{MSC}[3)]	–	–	ns	–
SOP/ENx outputs delay from FCLP rising edge	t_{45}	CC	-10		10	ns	–
SDI bit time	t_{46}	CC	8 × T_{MSC}		–	ns	–
SDI rise time	t_{48}	SR			100	ns	–
SDI fall time	t_{49}	SR			100	ns	–

1) FCLP signal rise/fall times are the same as the A2 Pads rise/fall times.

2) FCLP signal high and low can be minimum 1 × T_{MSC}.

3) T_{MSCmin} = T_{SYS} = 1/f_{SYS}. When f_{SYS} = 75 MHz, t_{40} = 26,67ns

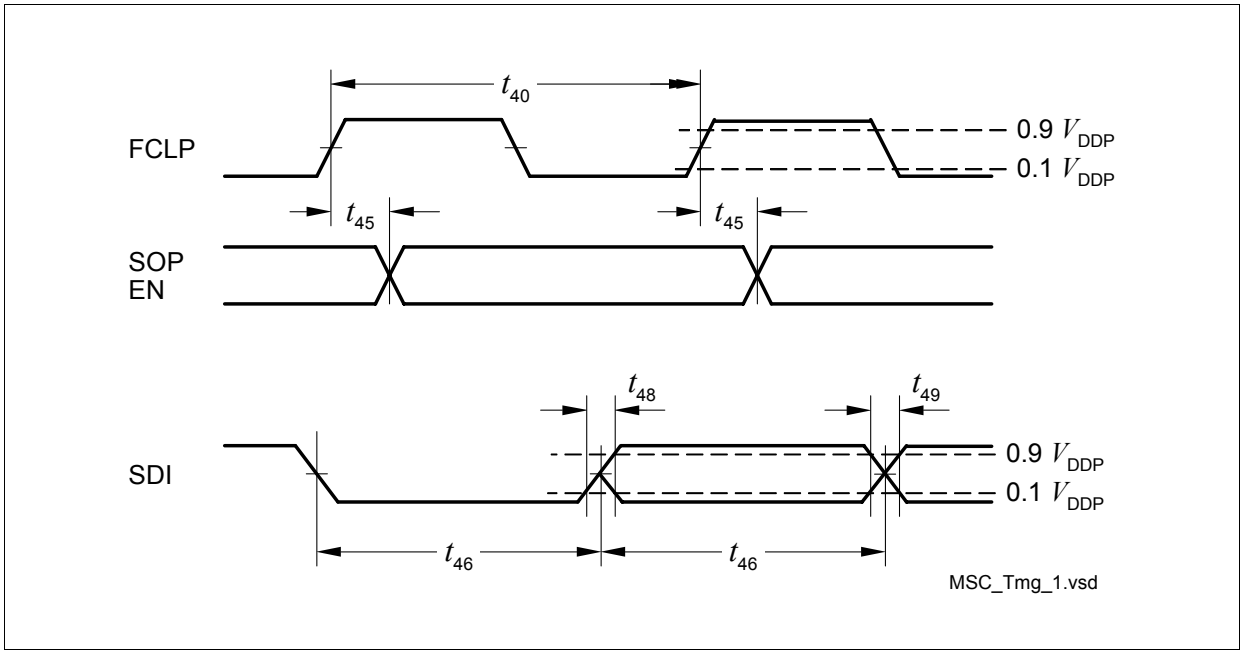


Figure 43 MSC Interface Timing

Note: The data at SOP should be sampled with the falling edge of FCLP in the target device.

4.3.12.3 Synchronous Serial Channel (SSC) Master Mode Timing

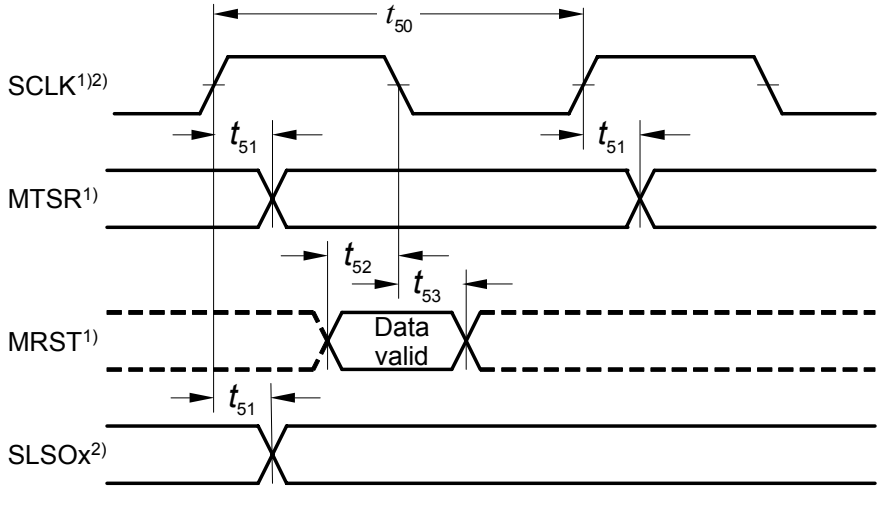
Table 34 SSC Master Mode Timing (Operating Conditions apply), C_L = 50 pF

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
SCLK clock period[1)2)]	t_{50}	CC	$2 \times T_{SSC}$[3)]	–	–	ns	–
MTSR/SLSOx delay from SCLK rising edge	t_{51}	CC	0	–	8	ns	–
MRST setup to SCLK falling edge	t_{52}	SR	10	–	–	ns	–
MRST hold from SCLK falling edge	t_{53}	SR	5	–	–	ns	–

1) SCLK signal rise/fall times are the same as the A2 Pads rise/fall times.

2) SCLK signal high and low times can be minimum $1 \times T_{SSC}$.

3) $T_{SSCmin} = T_{SYS} = 1/f_{SYS}$. When f_{SYS} = 75 MHz, t_{50} = 26,67ns



1) This timing is based on the following setup: CON.PH = CON.PO = 0.

2) The transition at SLSOx is based on the following setup: SSOTC.TRAIL = 0 and the first SCLK high pulse is in the first one of a transmission.

SSC_Tmg_1.vsd

Figure 44 SSC Master Mode Timing

5 Package and Reliability

5.1 Package Parameters (P/PG-BGA-416-4)

Table 35 Thermal Characteristics of the Package

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Thermal resistance junction case top[1]	R_{TJCT}	CC	–		8	K/W	–
Thermal resistance junction case bottom[1]	R_{TJCB}	CC	–		15	K/W	–

1) The top and bottom thermal resistances between the case and the ambient (R_{TCAT}, R_{TCAB}) are to be combined with the thermal resistances between the junction and the case given above (R_{TJCT}, R_{TJCB}), in order to calculate the total thermal resistance between the junction and the ambient (R_{TJA}). The thermal resistances between the case and the ambient (R_{TCAT}, R_{TCAB}) depend on the external system (PCB, case) characteristics, and are under user responsibility.
The junction temperature can be calculated using the following equation: $T_J = T_A + R_{TJA} \times P_D$, where the R_{TJA} is the total thermal resistance between the junction and the ambient. This total junction ambient resistance R_{TJA} can be obtained from the upper four partial thermal resistances.

5.2 Package Outline

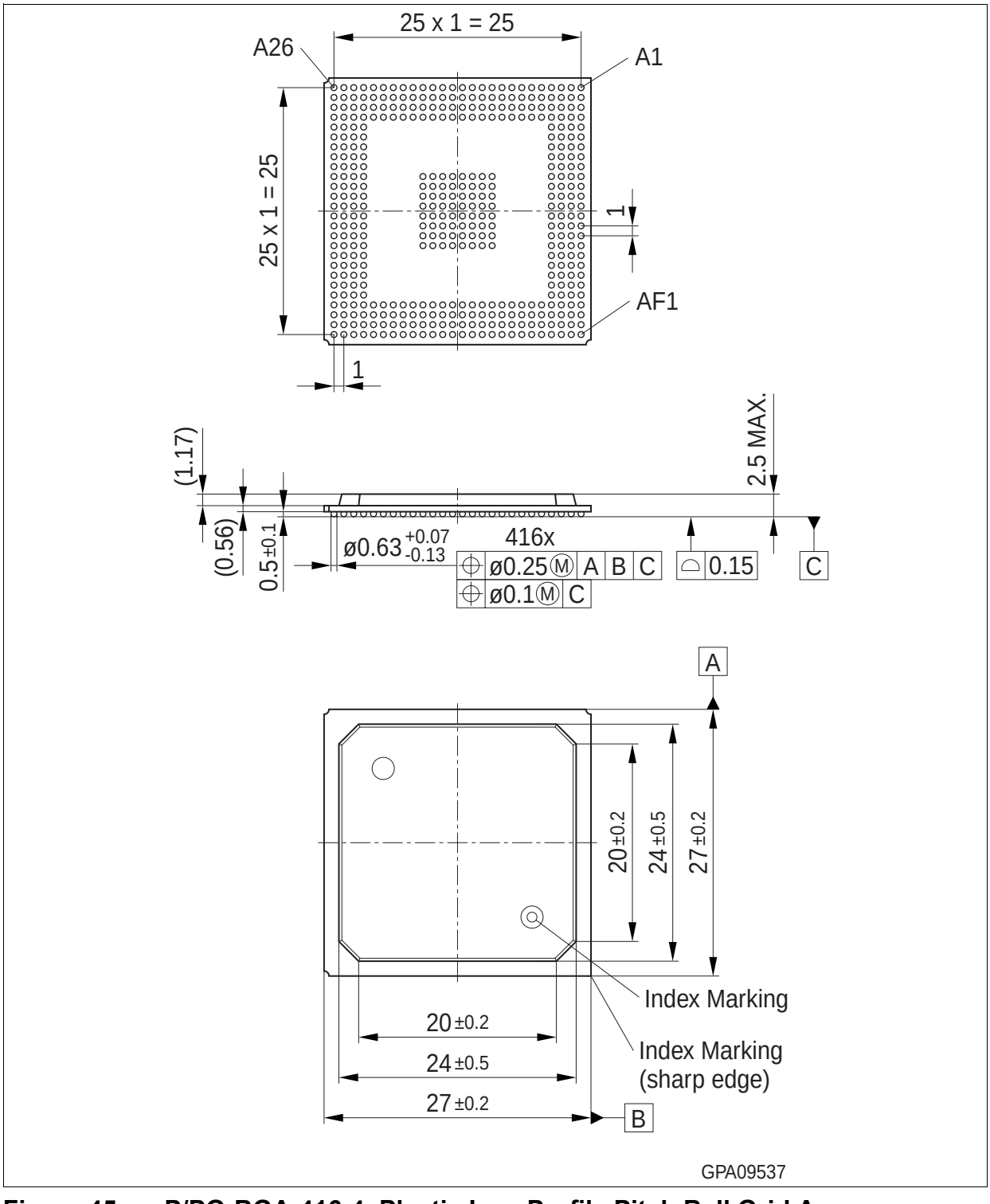


Figure 45 P/PG-BGA-416-4, Plastic Low Profile Pitch Ball Grid Array

You can find our packages, sorts of packing and others in our Infineon Internet Web Site.

5.3 Flash Memory Parameters

The data retention time of the TC1796's Flash memory (i.e. the time after which stored data can still be retrieved) depends on the number of times the Flash memory has been erased and programmed.

Table 36 Flash Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Program / Data Flash Retention Time, Physical Sector[1)2)]	t_{RET}	CC	20	–	–	years	Max. 1000 erase/program cycles
Program / Data Flash Retention Time Logical Sector[1)2)]	t_{RETL}	CC	20	–	–	years	Max. 100 erase/program cycles
Data Flash Endurance (128 KB)	N_E	CC	15 000	–	–	–	Max. data retention time 5 years
Data Flash Endurance, EEPROM Emulation (8 × 16 KB)	N_{E8}	CC	120 000	–	–	–	Max. data retention time 5 years
Programming Time per Page[3)]	t_{PR}	CC	–	–	5	ms	–
Program Flash Erase Time per 256-KB Sector	t_{ERP}	CC	–	–	5	s	f_{CPU} = 150 MHz
Data Flash Erase Time per 64-KB Sector	t_{ERD}	CC	–	–	2.5	s	f_{CPU} = 150 MHz
Wake-up time	t_{WU}	CC	4300 × $1/f_{CPU}$ + 40µs	–	–	–	–

1) Storage and inactive time included.

2) At average weighted junction temperature T_j = 100°C, or
the retention time at average weighted temperature of T_j = 110°C is minimum 10 years, or
the retention time at average weighted temperature of T_j = 150°C is minimum 0.7 years.

3) In case the Program Verify feature detects weak bits, these bits will be programmed once more. The reprogramming takes additional 5 ms.

5.4 Quality Declarations

Table 37 Quality Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Operation Lifetime[1)2)]	t_{OP}	–	–	24000	hours	at average weighted junction temperature T_j = 127°C
		–	–	66000	hours	at average weighted junction temperature T_j = 100°C
		–	–	20	years	at average weighted junction temperature T_j = 85°C
ESD susceptibility according to Human Body Model (HBM)	V_{HBM}	–	–	2000	V	Conforming to EIA/JESD22-A114-B
ESD susceptibility of the LVDS pins	V_{HBM1}	–	–	500	V	–
ESD susceptibility according to Charged Device Model (CDM)	V_{CDM}	–	–	500	V	Conforming to JESD22-C101-C
Moisture Sensitivity Level	MSL	–	–	3	–	Conforming to Jedec J-STD-020C for 240°C

1) This lifetime refers only to the time when the device is powered on.

2) One example of a detailed temperature profile is:
2000 hours at T_j = 150°C
16000 hours at T_j = 125°C
6000 hours at T_j = 110°C
This example is equivalent to the operation lifetime and average temperatures given in the table.

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